



## **Frequently Asked Questions**

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## Frequently Asked Questions

This document has been compiled over a period of time. As with all developments, constant feedback from users has deeply influenced the preparation of this FAQ list and will be upgraded and hoisted in the Net simultaneously. The Questions in this collection of FAQ have been organized under descriptive Chapters. For example, all Questions related to the PCB Layout Module falls under the Chapter titled **Layout Editor**.

FAQ on the following topics

**Installation**

**General**

**Schematic Editor**

**Layout Editor**

**Arizona Autorouter**

**Fabrication Manager**

**Library Editor**

**Mixed Mode Simulator**

**EDSpice Simulation**

**PCB Analyzers**

## Installation

**Q1: Please explain the licensing policy.**

The new licensing policy from version 1.10 and EDWin 32 version 1.40. allows you to install as many times as the number of licenses purchased. ie. Suppose you have purchased 2 licenses, you can install it on two different machines. Now if you want to install it in say your Laptop, then you need to uninstall one copy of the previous installations.

While uninstalling the license disk has to be put in the floppy drive. On successful uninstallation, the program increments the remaining valid installations one by one so that it can be installed on another system.

The program can also be uninstalled without keeping the license disk in the floppy drive. In such case one valid license will be lost. So we always recommend you to keep the license disk in the floppy drive during full uninstallation process.

You can install the program using the license disk supplied by our store or our authorized dealers / distributors only. If you copy the contents of one license disk to another it cannot be used for installation. The license cannot reside in a hard drive ie. installation can only be done from a floppy license diskette. We recommend you to take a backup of the license disk that can be sent to the dealer by email in the event of damage to the original diskette.

**Q2: I have copied the contents of the CDROM to a network drive since I don't use a CD drive but I can't seem to install it. Please help.**

Map the network drive before installation. However you will need to install your license from the floppy diskette.

**Q3: I am a licensed user but the program works only in demo-mode, the File → Save option is grayed out.**

This is because you have installed demo version. I.e. this happens when the path given for license during installation was the CD drive. Point the path to the license diskette instead.

**Q4: While installing on win95 OS, MFC40.DLL file does not copy the first time, a dialog box opens up asking to abort, retry or exit, when I press retry it copies the dll and continues.**

This occurs either if any Windows applications are open during installation or an older version of mfc40.dll may be present in that system. Close all operations before installation and allow the system to overwrite the older dll.

## General

**Q1: I am a new user, every time I try to do something it pops up a help window that I have to move out of the way, is there a way to turn this off?**

**Project Explorer → View menu → Uncheck Auto help**

**Q2: How do I get Windows like editing features?**

Select an object with Bullets (CTRL + CLICK). Right click to display the context menu. It is possible to Cut, Copy, Paste, Pack, Unpack, Change the X, Y position, change the reference, change size and literally do most editing operations in the property window which is displayed.

**Q3: How do I set the path to system files?**

The program creates its own default directories at the time of installation. The names of the sub directories (Sys, Lib, Job etc) cannot be changed during installation. However, the directories can be changed from **Project Explorer → System → Options → Files → Folders.**

**Q4: For better alignment of components, is it possible to change the small cursor into a crosshair cursor?**

Press Shift+Z to toggle between Long/ Short Crosshair cursors while performing an operation such as Relocate, Repeat, etc.

**Q5: Give me some information on the File type for Design (project) and library. Is it ASCII or binary?**

Design (Project) can be saved/loaded in ASCII format but not in binary. Library cannot be saved/loaded in any of these formats.

**Q6: I upgraded from Edwin to EDWin XP. It seems to work but, I can't open any design drawn in Edwin 16-bit version. What happened? Is there a way to transform my designs?**

Project Explorer → System → Conversion Manager

**Q7: How do I import a Spice netlist?**

Project Explorer → Project menu → Spice Netlist Import → Browse to \*.cir file.

**Q8: Can we use EED3 components in EDWin? Is there any way to convert them?**

Project Explorer → System → Conversion Manager → select the tab EEDIII Conversion.

**Q9: Can you please give a detailed explanation on hierarchy?**

Hierarchies are a way of splitting up and organizing large electronic projects into a systematic set of manageable small pieces. This is applicable only within the Schematic Editor.

Create the main Hierarchical symbol in Library Editor (Schematic Symbol only) and assign entries to it, submit it to the Search Sequence and load it in Schematic Editor. **Project Explorer → Project menu → Add Circuit → Enter name** of new circuit to be assigned to the Hierarchy in the text box, say Hier1 and click Accept to close this window. The additional circuit appears in the Project Explorer with its name in brackets. **Schematic Editor → Second function tool "Hierarchy Down"** | Click the main Hierarchical symbol. In the dialog which appears, select the circuit | Apply. Now the symbol is assigned to a circuit. Edit the page of Hier1 to find a net hook for each entry of the symbol. Connect the net hooks at the appropriate entries in the circuit. In case you make changes to the main Hierarchical symbol in Library Editor, do not forget to reassign the hierarchy so that the changes will appear in the circuit. **Schematic Editor | Second function tool Hierarchy Down | Second Option Tool "Reassign Hierarchy"**, click the Hierarchical Symbol and reassign the circuit.

All the hierarchies created will be listed in the Project Explorer allowing easy navigation between the hierarchies. The actual process of navigation is as follows: From the Schematic Editor select

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Tools | Components | Hierarchy Down. The option tools will now be shown. After selecting the appropriate one, click on any entry of the symbol you wish to view one hierarchical level down or up. (Remember that you can move upward only upto the level you have set as the current hierarchy). The Schematic Editor window will now change to show the schematic of one hierarchical level up or down, as selected. It is the same for EDSpice simulator.

**Q10: What is the difference between EDSpice and Mixed Mode simulator since EDSpice simulator can simulate circuits simulated by mixed mode simulator?**

Both EDSpice and Mixed Mode simulators can simulate both analog and digital circuits i.e. both are mixed mode simulators. Mixed Mode simulator is the native Simulator of the package while EDSpice is based directly on Berkeley SPICE 3F5 and XSPICE from the Georgia Institute of Technology. In addition to the XSPICE extensions, EDSpice continues to support capabilities and models of SPICE2. This is specifically meant for users who are familiar with Spice.

**Q11: Why do I have problems while working with Postscript printers in Windows NT and 2000?**

While printing from EDWin32 and EDWinXP using Postscript drivers, the system cannot print the lines in the precision (true size) specified. This is a known problem in Microsoft Windows NT and 2000 and it is mentioned in their technical documentation. We have tested this with a postscript viewer, and the result is the lines are very thin line rather than in true size.

To overcome this, use Win95/98 kernel in which we have explicitly handled these situations for printing (only)

1. Take a backup of EDWinXP/Edwkrn2k.dll.
2. Copy the file Edwkrn2k.9x\_ and rename it to Edwkrn2k.dll and place it in the /EDWin folder
3. Carry out the printing job.
4. Rename the 9x kernel to its original name "Edwkrn2k.9x\_", restore the original Edwkrn2k.dll.

"ActiveX can't create object" error in Waveform Viewer

**Q12 : When I try to open Waveform Viewer, the following message appears: " ActiveX component can't create object". My Operating System is Windows 98.**

This is because DCOM is not updated in your machine. The Waveform Viewer will start working by executing the CDROM | Tools | DCOM | DCOM98.exe. For those who are using Windows 98

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SE, please visit the site [http://www.microsoft.com/com/dcom/dcom98/dcom1\\_3.asp](http://www.microsoft.com/com/dcom/dcom98/dcom1_3.asp) .and download it. This issue remains unresolved for Windows Me though Waveform Viewer will work if updated with the file supplied with the CD. This file however, is meant to be used in Win9x machines. We are not aware of the conflicts which will arise by using DCOM98 in Windows Me.

**Q13: Adding related projects**

Can I merge two existing projects into one, each project having its own Schematic and Layout representation. I would like to integrate the Display Unit of my electronic project and the Control Unit into a combined project )

It is possible to add an existing circuit of one project to another. Save the Display project as a circuit (Right click on CIRCUIT menu in Project Explorer and select Save Circuit | a Save As dialog appears | give the circuit a suitable name, say Display. Now open the project where this circuit has to be added and select the Project menu from the Project Explorer, right click and select Load Circuit. Select the Display circuit.

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## Schematic Editor

### Q1: How can I make my working sheet large enough to draw a big schematic?

The page size may be redefined using **Tools | Page format | Define Page**.

Otherwise draw the rest of the schematic in a new page using **File | New Page**.

The maximum acceptable size for a page is 4 x 4 meters and the maximum number of pages that can be used in the Schematic Editor is 99 pages.

### Q2: In Schematic Editor, after a circuit is drawn, we autopackage. Can you explain what is actually taking place in autopackaging and why?

The autopackaging utility allows performing the automatic packaging of all unpacked components and it assigns the first free number to the last placed components belonging to the same group. The component name prefixes from Part descriptions are used to automatically generate component names.

During packing system extracts the package assigned to the part at the time of creation. This is how it displays the respective package facilitating front annotation.

Note: After Autopackaging if any components are deleted, then select **Project Explorer | Project menu | Compact Project Library** to delete unused components to avoid irregular numbering of components or corruption of the project.

### Q3: Concept of nets and wires

Net is a collection of nodes that are electrically connected together. A wire is merely a visual representation of the corresponding net description. The creation of a wire automatically results in the creation of the corresponding Net. Further, the deletion of a wire removes only the wire but does not remove the Net whereas the deletion of a net removes ALL the associated wires. The deletion of a node in the net removes the corresponding connection in the net and removes the associated WIRE SEGMENT/ TRACE SEGMENT also.

It is possible to delete a wire and the corresponding net connection together using **Tools | Nets | Delete a Node**. This will delete the associated **Wire Segment/ Trace Segment** also.

**Q4: How do you print the schematic hierarchy contents?**

Select the specific schematic hierarchy from the list of hierarchies. Use **File | Print Page** in Schematic Editor to print the schematic hierarchies.

**Q5: How do you change the thickness of wires?**

The thickness of wires & buses can be changed even after routing using either of the following methods.

a) Invoke **Options | Sizes | Schematic | Bus/Wire** from the task **System** in the **Project Explorer**.

In the edit boxes provided for bus and wire line width, change the value.

Now to effect this change as the default setting, select the **“Save & Exit”** from the



dropdown button before exiting from this window.


**Note:** If this change is just for the current project, then click the APPLY button and exit.


b) Use **Project | Project Properties | Advanced** to vary the Wire thickness, Symbol outline etc. by value or by percentage.

**Q6: When I use "redraw on component" in Schematic, an error-message "component not found" appears although the component is apparently there in the schematic.**

To zoom on 7474,1 that is packaged as U1, enter U1/1 (i.e. specify the group number) to redraw it in schematic. But in layout only the name U1 is needed.

**Q7: About Merging and Splitting of Nets: I am not able to split and also end up in merging the nets which I don't want to?**

Splitting nets is a very simple process. Select the tool  Split Nets from the Wire/Bus toolbar. Click on the wire, the entire net gets selected. Click once again on the same wire, this pops up a window, enter a new net name (system automatically inserts the first free number) and check

“Named ” in the window. Accept the new net name and verify using the tool  Wire/ Bus Property.

But the system won't allow splitting a net that has only a single branch as shown in Figure - 1.

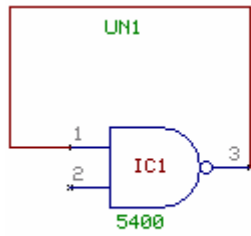


Figure 1

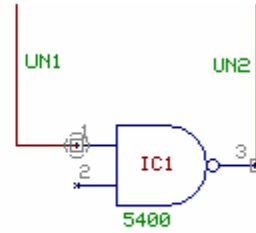



Figure -2

To split such a net, you have to delete a wire segment so that two or more branches exist in the net as shown in Figure - 2. Now select any node in the net and the system prompts to select the next node in that net which is to be splitted.

To merge, invoke the tool  **Merge Nets**. Select the net you want to merge and click on the other net. A confirmation prompts. Now click YES to merge two nets into one.

**Q8: I made the schematic diagrams and the layouts for an audio pre-amplifier and amplifier in 2 different projects. Is it possible to merge the two diagrams to create one single schematic diagram and layout?**

It is possible to combine two **Schematics / Layouts** using **Tools | Block Edit | Block Save / Block Load** facility available in Schematic and Layout Editors.

**Q9: I created three busses with different names A, B and C. Then I suddenly discover that two of the busses should have the same name. Is there any easy way to change bus name without deleting it and rewriting it again, because when I try to rename C as B, the system says that B already exists?**

Merging of two existing busses is not permitted. The only possible way is to give similar names at the time of bus creation. For e.g.: create one Bus and give names as B and create another bus and give again B.

**Q10: I tried to copy a schematic to a Microsoft word software, (zoom1: 1), and I got half of the picture in my word document. When I copied the schematic to the clipboard (zoom 2:1) to Microsoft word document, I got a very unreadable picture in the word document. Please tell me, is it a different way to copy schematic to word document and still to read the schematic in the word document.**

Use **File | Copy Screen** to Clipboard or "Ctrl+C" to copy the currently viewing part of the diagram (work area). Then paste it to bitmap editor and load this bitmap to word document. Otherwise directly paste it to the Word document without loading to the bitmap editor. To copy full screen/ highlighted window handle use basic Windows operation such as "Print Screen" | "Alt+ Print Screen".

**Q11: I cannot find a method of searching for an item. E.g. a resistor. I would like to search for, say R234 and have it highlighted in some manner in the schematic and the layout (perhaps elsewhere too) - is there a way to do this?**

Use CTRL+F combination key to pop up a component information dialog. Select the required tab and double click on the entry or component to redraw it on the workspace.

**Q12: How do I search for a particular net in a project?**

To search a particular net from the project, select **Tools | Nets | Net property**. Click on the free workspace and enter the exact net name to highlight it on the page/board as well as to open up its property window.

Otherwise use CTRL+F (refer Q11).


**Q13: Can I set the component values in schematic?**

Use **Tools | Components | Add /Change component text | Add /Change value**.

**Q14: Can components be rotated in 10 ° steps?**


It is possible to rotate a component in any step greater than 0.01°. Enter the required angle of rotation in the dropdown 'Angular Snap' (Standard Toolbar) and then rotate the component. Otherwise specify the angle of rotation in the component property window.

**Q15: How can I stop the Bus member number sliding, when I delete a net, that is bus connected with a defined bus number? I wish that the other nets in bus held their previously defined bus member numbers.**

If you are deleting the whole net which is connected to the bus by selecting the tool  Delete whole net, then on redrawing the circuit the bus member number also gets renumbered. This is because on deleting a net, the part once again gets repacked and it renumbers the bus members also.

More on Bus member number

Bus member number allows to group nets having the same bus member number, So it is advisable to have default numbers (0,1,2...). If the default bus member number (e.g. 0) is to be

changed, then select the tool  Add Net/ Bus Labels from the Wire/Bus Editing toolbar and click on the bus member number. In the window, enter the required name (D0) and click O.K. Now click on all the bus member number having the same bus member number (0) and assign D0.

#### **Q16: How can I make Pin numbers of a new symbol visible in different Editors?**

Edit the symbol in the Library editor and check PA Texts from View menu. Position the PA Text and select the "Edit Entry Attributes" tool. Now click on each entry and check the "Visible Pinout" check box. This will display the pin numbers in the Schematic after the component is packaged.

See that in the Packaging Preferences, the option to view the pinout is checked. To check this option, select **Project Explorer | System | Options | Packaging Preferences | Pinout**.

Now to effect this change as the default setting, select the "Save & Exit" from the



dropdown button before exiting from this window.

Note: If this change is just for the current project, then click the APPLY button and exit.

#### **Q17: I autopacked a schematic and all four opamps went into four separate IC's. Then on trying to get them into one IC, I find that I cannot individually pack the op amps. How do I sort this out?**

**This could have happened in the following way:**

For e.g.: LF147 contains four schematic symbols OPAMP, OPAMPA, OPAMPA, OPAMPA. To load the part LF147, open the library browser and search for the component LF147. When you drag and drop this component on to the schematic, you get another input box with a drop down list. Select the symbol OPAMP. When **Accept** is clicked OPAMP is loaded. If this step is repeated again, another OPAMP symbol will be loaded. Now packaging the symbols will load two ICs of device LF147 in the layout. This is because device LF147 contains only 1 OPAMP. On the other hand, if you select OPAMPA from the symbol dropdown list while loading the part LF147, and

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then package, you will get only one IC in the layout since a single LF147 contains OPAMP and OPAMPA. The function tool Repack allows repackaging an already packaged component.

**Q18: After routing there may be wires that are not routed. It is difficult to see precisely where these nets go. When I click on one node it simply gives me the net name and details of the component. Please can you tell me how I can identify the unconnected nodes and display the information.**

There is no special tool provided for viewing the unrouted traces. But this can be checked using the menu **Info | General | Nets**. The Net Map window lists all the nets in the project and the right side window shows the components in the selected net. Select one net from the left side box. If the net is properly connected using wires the column 'Status' will show "Connected".

**Q19: When I tried to print Schematic, I found that the default line width of 0.0020" meant that the print was not clear that would not fax satisfactorily, so how can I to give a better definition to the symbol line width.**

Use **Project | Project Properties | Advanced** to vary the Wire thickness, Symbol outline etc. by value or by percentage.

**Q20: Is there any way in which I can selectively pack a few components at the same time irrespective of their prefix?**

This is possible in different ways.

a) Bullet/ Select the components which have to be packed (Ctrl + Click) | Right Click | Properties | Schematic Component | Select "Schematic Components" | Right click | Pack. Similarly, it is possible to Unpack and Repack.

b) Info | General | Select Tab "Sch. Components" | Select the components to be packed (Ctrl + Click for non consecutive selection and Shift + Click for consecutive selection) | Right Click | Properties | Select "Schematic Components | Right click | Pack.

**Q21: I miss the feature of changing the reference of a component which was available in previous versions, I can't find the function tool?**

Library Explorer | Alt + Drag Drop the part to Schematic/Layout component whose reference has to be changed. Alternatively, bullet the component and change the name of the part in the property window.

The same applies to Layout Editor. To change reference of packaged components, reference has to be changed in the Layout Editor.

**Q22: I get the error message “Cant load Part XXXX” and “Can’t find part XXXX”.**

Make sure the part library is submitted to the search sequence. Library Explorer | View | Search Sequence

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## Layout Editor

**Q1: After Schematic Editor, I opened the Layout editor, but Packages does not appear. In Layout editor I don't see anything, only PCB frame. What's wrong?**

After placing the components in Schematic Editor, they have to be packed. Only then will the packages become visible in Layout editor, and they will be all positioned at the Board Datum. Relocate one by one (use redraw to make the next part visible) on the board or do Autoplacing.

**Q2: How can I add text outside the board outline, indicating layer of the particular artwork, to my PCB design?**

Select Layout Editor | Tools | Texts | Create Text. Click on the workspace. Type the text in the window that pops up and place it outside the board outline. (before creating the text, select its placement layer using the menu, Layer). The placement layer of an already created text may be changed using the tool Text Property from the toolbar. Now, in the Fabrication Manager module, generate the GBR file for the particular layer. Preprocess the GBR file to an artwork file. Now in Tools | Gerber view you may view the text created placed above the board. In case a text string, which is not needed in the artwork, but is required to appear only on the screen, use Tools | Notes in the Fabrication Manager module.

**Q3: Can we have a utility that hides the comp. Name in the module layout?**

Tools | Component | On/ Off Component name.

**Q4: Will a click on an incomplete trace result in a finish of that trace (as it should) or does it make a new trace with all the possible errors involved?**

The program will assume a click on an incomplete trace as a new trace element. Clicking on the incomplete trace with the tool 'Allow T-Connections' enabled will create trace element as the part of the same NET. Without selecting this option, it will create a new NET.

**Q5: What are branches?**

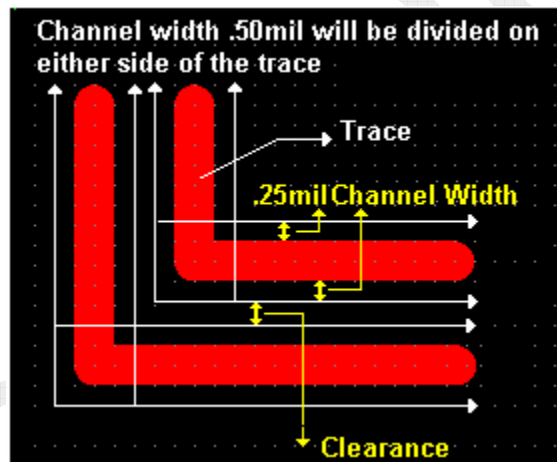
Branches refer to the portions of a single net that is physically connected with two or more parts.

**Q6: When connecting a trace on the component side to a component with legs, the trace is connected to the component layer pad. Is this pad connected to the solder layer pad on the other side of the board? Or a via should be put in?**

For a through hole components (PMD) pads will be in all layers and it is not necessary to connect to solder layer or through via pad.

**Q7: Can you define Channel Width .How can I do the clearance check? If I have a 10 mil trace, and a channel width of 25 mils, what will be clearance to the next trace?**

Channel width of a trace simply means that the system should reserve an area for that trace. i.e., if you have a 10 mil trace, and a channel width of 25 mils, 12.5 mils ( $25/2$ ) will be reserved on either side of the trace. i.e. A total of  $12.5+10+12.5$  mils will be reserved for the trace.



**Q9: How can I locate the center of the padstack for the purpose of routing? Can I use a full screen cross on the cursor?**

You can use full screen cursor. Press Shift+Z to toggle between Long/ Short Crosshair cursors while performing an operation such as Relocate, Repeat, etc. To confirm the selection of the pad is to use F3 option tool while routing. This option allows only pin to pin routing. To continue with free routing, disable F3 while routing and enable F3 at the time of connecting to the pad.

**Q10: How can you display the ratsnest of the net being currently routed?**

Preferences | Guidelines [Net] shows the ratsnest for the net being routed.

**Q11: I made a square copper area on the component layer, just for cooling purposes. But I only see the outlines the area is not filled. Could you please help me with my problem?**

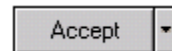
Create the copper area along with 'Filled item' tool selected. Make the View | Layout | True size ON to get the filled effect.

Note: Filled option is available only for regular shapes. For irregular shapes, use copper pour area.

**Q12: What does AGAP do and what is it for?**

Agap is the minimum electrical insulation required for a trace, pad or for a copper item. Only the traces currently being routed take the Agap value that has been set in the Agap combo box. All other traces continue to take the default Agap setting. In order to change the default setting of Agap to the one desired, select Options from Project Explorer and choose Sizes | Layout | Airgap. Here, the airgap widths for trace segments, Round & square pads can be set.

Now to effect this change as the default setting, select the "Save & Exit" from the



dropdown button before exiting from this window.

Note: If this change is just for the current project, then click the APPLY button and exit.

**Q13: I have a board with several hundred pads and I want to change their size graphically. Can you please tell me how to do this without deleting and recreating them all?**

For this you have to make changes in Packages. Select a Package to edit in Library editor. For changing the padstacks select the tool "change padstack". Use the option tool F1 to select an existing padstack in any padstack library or F2 to create a new one. Then click on the required padstack in Package to be change it to a new one.

Note: Block select for multiple replacement with new padstack.

**Q15: Does the software allow thermal pads for SMD and PMD (through hole)?**

It is not possible to create thermal pads for SMD. For PMD (through hole) the system will automatically generate HRF (thermal pads). Actually there is no need of HRF items in SMD. If you are so specific about it you can create it manually. See Tutorial for how to create padstacks.

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**Q16: I am trying to import a dxf board outline but it keeps hanging with the busy light on. Why?**

There are certain conditions that must be kept in mind before importing .DXF files.

Some of the conditions are:

- 1) Issues an error message "Board outline is not closed at x,y", if the created Board outline does not enclose an area.
  - 2) Accepts board outline created only in single layer from AutoCAD.
  - 3) Allows importing board outline created only with arcs, lines and polylines
  - 4) Does not consider board outline created with double lines and arcs (i.e. Multiple lines created in AutoCAD enclosing an area) using a single tool though it encloses an area.
  - 5) Relaxes board outline to be created upto a maximum of 32000 x 32000 mils or 32 x 32"
- May be the dxf file which you are trying to import may be overriding any of these conditions.

**Q17: Can I create a copper pour area that is Hatched?**

Follow the steps below:

Create copper item using circle or rectangle.

Next enable the function tool "Hatch Copper" and choose the option tool F3 i.e., "Select items" tool and select the copper items that are to be hatched.

After finishing the selection enable the option "Execute Hatching" (F1) tool. Now click on the working area to invoke a dialog box in which the hatch pitch may be entered. Here we have entered 0.1".

Click OK and return to the workspace. If you have enabled the option F2 then hatching will be performed at 90°. If you turn off the True size view you can view the hatches.

**Q18: In Layout Design, is it possible to move a block of components on only one layer while still have all other layers visible?**

Tools | Block edit | Relocate by Vector

**Q19: How can I place Test points on the PCB in the layout editor?**

Use Tools | Components | Open part library | Add test point with through hole to place a test point on any layer on a trace. If the user wants to place the test points on the top and bottom layers only, select Tools | Components | Open part library | Add test point on surface layer.

**Q20: Is it possible to adjust via diameter?**

Layout Editor | Tools | Via Padstack (before coming to this option select the required padstack in settings panel ie. #1 to #7) | Give necessary values for editing | Accept.

The Via Padstack can be edited prior to designing the board. This is done by using **Project Explorer | System | Default Via Padstack Editor**.

**Q21: Is there any troubleshooting utility which will check the project integrity , detect errors and fix it?**

**Layout | Auto | Net Trace Integrity**. This should be done when there are crashes while doing net or trace editing operations.

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## Arizona

**Q1: Some parts of my layout have to be routed manually, because there are high voltage sections on the design. Is it possible to 'tell' the Autorouter, that some regions of the PCB should not be routed?**

Layout Editor | Tools | Board Outline | Define outline | Create Router keep-off zone

**Q2: Is there a way to define the width of traces in power and signal nets?**

To define the width of traces in power and signal nets, proceed in the following way:

Select the option tool 'Routing nets Parameters' from the function tool 'Parameters Setup'. A window 'Net Parameters' pops up. The Width and Via set as default for Power and Signal lines are displayed. Define the required value and click **Accept**. After autorouting, when you export back to Layout Editor, your traces will be routed with the defined trace widths.

**Q3: Is it possible to specify all traces to be routed to components, through the solder side only?**

At the time of autorouting specify the layer(s) on which routing should be done. There are options for specifying these layers in the Arizona autorouter.

Select the tool 'Select Layers and Directions' from the toolbar. A window, 'Settings' pops up. By default the setting will be as follows: -

Component Layer - Horizontal direction (both power and signal lines)

Solder Layer - Vertical direction (both power and signal lines)

To restrict trace routing on the component layer click on the column 'Direction' of the component layer. The direction gets changed to Vertical. By double clicking once again the layer gets unselected. Disable all other layers. Now, the only layer selected for routing will be the solder layer. Perform autorouting with this setting.

Now, if there are unrouted pairs, you may have another iteration of the routing process with the direction for the solder layer changed to Horizontal. In order to get the best results adjust the routing parameters to suit to single layer routing. Obviously, in the case of very complex boards, single layer routing may result in unrouted pairs.

**Q4: In some complex circuits, the traces are missing when AutoRoute is given? Why are they missing and how do you overcome it?**

In complex circuits, it may happen that autorouter is unable to route all the traces with the set strategies and parameters. In such cases, you will have to manually route the remaining traces or else change the parameter settings such as decrease the wrong layer cost thus giving the AutoRouter more flexibility of routing. Once you have prerouted your board, with orthogonal traces, you can prevent rerouting by Autorouter by selecting load Load Options | Fix prerouted traces from the File menu.

**Tips**

In Autorouter, set the layers before routing. On each layer two ways of routing may be done i.e. horizontal and vertical. You may pour copper to prevent autorouter from routing.

**OR**

The other way is to give directly for Autorouting after setting the layers, then view the list of unrouted pairs and route these pairs manually.

**Q5: In the Layout Editor, after using the autorouter, I routed manually some orthogonal traces. But when I want to use the autorouter again my last traces don't appear. What is the solution for this?**

Autorouter loads only traces which starts and ends on pads. Any manually routed hanging traces, and traces that end on other traces, will not be loaded by autorouter. So please take care to route only traces from pad to pad if you are routing some traces manually before invoking autorouter.

**Q6: How to convert 16-bit strategy files to 32-bit strategy files?**

You cannot use 16bit strategy file to 32bit by simply renaming the .bs to .rsf. This doesn't make the conversion of strategy file. Either you have to convert this strategy through the database conversion using Conversion manager or you have to generate a similar strategy file and save it to .rsf file. In the first case the strategy file get converted along with the database and thus you will get it in the Arizona Strategy window. Here you can save the file by clicking "SAVE" button and it gets saved to .rsf extension file.

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**Q7: When I start my autorouter and I try to load the layout into it I get next error code: Error code= 409, Error func= 403, error padstack. What does this mean and how can I solve the problem so that I can run the autorouter?**

This error indicates that there may be some problem with the padstack. Either it may be created incorrectly or you might have placed it in the wrong way. Please check all the padstack in that particular project.

**Q8: I try autorouting the layout design using Arizona and a blank board is displayed. I also tried to load the file but get the following message: "ErrorCode = 404 ErrorFunk =300 Merge nets in the board? What must I do to comply with this message and prevent the same situation again?**

The problem is due to the multiple assignment of a single pin to the nodes for some parts. Arizona is pointing out this error while loading. To figure out the Part, which has multiple assignment of pins, take Library editor. In the table that shows the pin assignment, find the pin that is assigned to two nodes. Follow the same procedure and check for all the parts that are used for the project.

Immediate Solution:

Delete one of the assignments for the pin.

When you invoke Arizona from layout it just loads the Screen with that layout, actually the project is not loaded in this condition. In this case, Arizona routes blank traces on the board. Select File | Load board to Route from project to actually load the database.

**Q9: To route traces in Arizona Autorouter between two TQFP packages. I could route between SOIC and DIP packages but that seems impossible with TQFP parts? Give a solution?**

You can use different strategies for better autorouting. Arizona | Strategy | click on Load button | SMD.RSF, select SMD then click on RUN button. Now you will be getting better routing. You can also create your own strategies. For more details please refer help files.

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## Fabrication Manager

**Q1: When selecting “Define artwork”, is it necessary to select mirror at the solder layer? When should we use the mirror?**

If you select mirror, you will be able to view the solder layer as when you look at the PCB from the solder side. Otherwise, you will be viewing it as when you look at the solder layer from the component side.

**Q2: How can I blend (carefully) the component print layer with the component trace layer (so that I get the names etched out) Is there a way to do this? I'd like to remove the component outlines and leave just the names?**

This may be achieved as follows:

- 1) Load the project, invoke Library editor and remove the component outline from all the packages
- 2) Using Layout Editor you can switch off all the COMPNAME text on the board.
- 3) Add COMPNAME text in component layer using Tools | Texts menu in Layout Editor. (Step 1 and 2 may not be carried out if you decide just to discard the print layer. But the board may look displeasing with duplication of COMPNAME text in print and component layers after 3rd step is carried out. )

**Q3: Can I generate heat relief pad in fabrication manager or in layout editor? If yes, how?**

You can generate it in Fabrication manager. Heat Relief Pads are used mainly for two purposes:  
To arrest the flow of solder within the internal layers while wave soldering is done.  
To allow heat dissipation.

The procedure is as follows. Select Copper Pour Area tool from Create Copper graphics item in Tools | Copper mode. Select the layer and the net (or else last created net will be taken). Draw the boundaries of the Copper pour and finish. The option of Stretch item tool allows you to edit Copper Pour Area. Now invoke Fabrication | Setup | Gerber Artworks. Select the layer and click execute to open up another window. Here click EXECUTE to start processing. Now select Gerber viewer Setup from File menu. The Gerber files are to be selected in the order given below to get a



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Program checks several things and issues warnings or refuses to process.

**Q6: How can I print out the layout with drill holes in the pads? (via's and components)**

From the Fabrication Manager, select **Tools | Artwork&Pwr/Gnd planes |** Select layer for display. Enable **View | Artwork | Center holes** then go to **File | Print**.

**Q7: When I took a printout of the layout, pads appear smaller than on the screen. Why?**

Load the project, invoke Fabrication Manager and select **File | Print**. This pops up a window that displays a sheet outline. As the scale factor is changed, the system automatically computes the scaled size of the print and displays in the picture size. When this picture size is more than the printer paper size chosen, a page matrix overlapping the drawing outline is displayed. The number of pages to which the drawing is split is indicated by this matrix along with the number of sheet information at the bottom of the matrix. By default the print scale will be 1:1. That is the reason why you are getting the pads in small sizes. Set the above-mentioned print scale. Try this method and check whether you are getting the pads in the required size.

**Q8: How to view mechanical details in Gerber file? I can't find the file.**

You can create mechanical details in Gerber file using **Tools | Notes, Create Graphic Item | Create Text**. Then, select **Fabrication | Setup | Gerber Mechanical Plot** enable the check box **Board Description** and click **Execute**. By default the created Gerber file has .GBR extension with the first six letters of the file name being the first six letters of the project name and the last two being 90 for component side and 91 for solder side. Now view the generated artwork file in **Tools | Gerber View**. Mechanical plot may include board outline, dimensions, board description notes, holes and pad frames.

**Q9: Can we adjust the size of pads in Fabrication Manager? If yes, how? When we sent the Gerber data to photoplotter, can the size of pads modified be recognized by the photoplotter? If yes, how does this happen?**

You cannot make any adjustments to pad sizes in Fabrication Manager. Editing operations has to be done in the layout.

The de facto standard for photoplotter data is Gerber format. While generating Gerber files, these pads will be converted to Gerber format. These Gerber files are generated using the aperture

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sizes available in the Aperture Table. These apertures are defined in terms of a format recognized by the photoplotter called Dcodes. All the available Dcodes and the sizes they represent are listed in Aperture Table. The interpretation and repertoire of Dcodes may vary depending on the make and model of the photoplotter. For example Dcode D100\* may result in one machine as a .062" line and on another as a .100" line. There are photoplotters that allow flexible Dcode to aperture assignment. For certain others the repertoire of Dcodes may be fixed. Latest photoplotters available in the market may recognize various Dcodes for creating different shapes. There are three Dcodes for each available aperture size, namely for plotting lines, flashing round pads and flashing square pads that are recognized by almost all-standard photoplotters.

**Q10: While testing connectivity of the artwork, I get a "possible unroutes" error. After I poured the SPL0 copper, I get two wires as "possible" unroutes. Is this a via problem? Or an airgap problem?**

This warning shows those nodes of the selected reference net that are not connected to the poured copper. Connectivity Check in Fabrication Manager verifies that the pads included in the selected reference net are properly connected to the poured copper and checks whether any of the other nets are shorted to the poured copper. Suppose you have defined SPL0 in the component layer and are also referring this net for copper pouring. Then the list of possible unconnects just warns you that certain nodes in the net are not connected to the copper. It doesn't mean that these nodes are logically unconnected. If a part of the net is routed in the solder layer and you select any node of this net, then again, this warning get displayed with the nodes on the solder layer highlighted.

Note: Remember that this artwork check considers copper pouring for the selected layer only.

**Q11: How is it possible to print realistic pcb's on a laser jet? The holes dimensions are much bigger than the original size?**

**View | Artwork | Centre Holes** menu allows to select three hole sizes viz. 1/1, 1/2, 1/3. Select these options as per the requirement and select **File | Print**.

**Q12: How to copper fill over tracks and have a clearance between the copper fill and the tracks (feature)?**

Invoke **Fabrication Manager Tools | Copper** menu item and pour copper using the tool "**Create copper graphic item**". If you want to pour copper over the tracks you can do it using this tool.

You can change the copper to selected net using the tool "**Change net assignment**" after selecting the particular net from the "Net" drop down item in the toolbar. The clearance between the trace and the copper will be the airgap. You can change the airgap of the trace before routing. Change the Airgap (from toolbar) and then route the trace.

**Q13: Is there a possibility to generate automatically a ground plane? If no, can I generate it by growing the width of the track?**

The system will not generate ground or any planes automatically. You can make this by growing the track size. But it is suggested to use copper pour or use one plane itself for connecting grounds.

**Q14: What is the procedure to get a negative layer in files with the center hole in it and to print to my laser printer too?**

If you want a negative plot for a layer, please do the following steps:

Select **Fabrication | Setup | Gerber Photoplotter Data | Gerber Artworks**. Set the artworks for the selected layer by clicking on particular layer. Click the Execute button. Now in the Gerber-Output window which pops up will list the positive as well as the negative plot of the selected artwork. The Negative layers starts from \*50 onwards. Now preprocess the layer selecting from File | Gerber Viewer setup and select Tools | Gerber view to view the negative layer.

**Switch ON View | Artwork | Centre holes**. Now you will get the negative layer with its center holes. To print, select **File | Print**.

**Q15: How can I print a block or draw lines on the Comp.Print layer? I have been trying many things in both Layout as well as Fabrication Manager but cannot get the lines/ block when I create my Gerber files.?**

Invoke Fabrication Manager, **Tools | Notes** and select the tool Create Graphic item. From here you can draw lines, arcs, blocks etc. This will be effected only for Print layers. To get this in Gerber view you have to select **Fabrication | Setup | Gerber Photoplotter Data | Gerber Mechanical Plot** and select the layer and execute it. And view that particular layer in Gerber view (Tools | Gerber View). The notes should be placed well within the board.

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**Q16: What is the hole category? If I use the value 0, it is OK and perhaps without larger meaning in normal use?**

It is possible to group holes into a maximum of 8 categories depending on their type. Type, here, implies whether the hole is to be plated or not etc.

**Q17: Is it possible to print out the D-Code Gerber Aperture table?**

You may open the \*.APT file (residing in the ..\Sys directory) in notepad and take a print-out.

VISIONICS

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## Library Editor

**Q1: Please tell me if I can take a print out of the library list (all or a part of it).**

You can print the list of parts; its associated Symbol, No. of groups of Symbol and Package (name of component used), using the List Generator (Right click on the task, System in the Project Explorer to popup a list of functions). Click on List Generator to launch this module.

**Q2: I would like a part library in the ../ Lib folder to be available for the search list just as the other supplied libraries.**

Once you have created the parts, save the part in the library. Select the path ( ../ Lib if that is the path you need) and enter the new name of the \*.PART file in the text box (say MINE.PART) under the path selection box. Now click on SAVE. You can save all your new parts to this new PART file. To include this newly created part file in the Search sequence, select the View | Search Sequence menu from the Library Browser/ Library Explorer and check the files that have to be included in the Search list explicitly.

**Q3: I built a simple schematic with IC's from the library that I built. The problem is that when I tried to build a layout, the SLP1 & SLP0 net was not connected to any of the ICs. I checked the parts everything looked just fine. Any idea what's going on?**

If you load ICs from the Library, it should have SPL1 and SPL0 nets already assigned. You can see this in the Library editor window. For the part you created, you should assign SPL0 and SPL1 explicitly for the pins, which are to be set as Gnd and Pwr nets respectively, during creation in Editor. Load these to the Schematic, package them and then invoke layout. Now you will get the ICs in the Layout. Select **Info | Nets** to view all the Nets that are already assigned. You should get SPL0 and SPL1 there.

**Q4: I'm working on a layout where I need to arrange 15 LED's in a circle, with equal distance between them.**

Create a symbol as said below and load this as symbol in layout. First measure the LED width between its two ends. Now create a line of that length and place it. Create a contact point (Select point P1) to define the rotation of the line. Using the rotate and repeat option tool click on the line. Enter the no of lines to be created and the angle ( $360^\circ/\text{total no of the item}$ ). You see that you get a circle. Now relocate the default pad (or change the pad) at one end of the line. And once again define the rotation by placing a contact point. Click on the pad with the rotate and repeat option tool. Enter the same value as above. Create another pad and place it on the other end of the line. Rotate and repeat this pad as explained above.

**Q5: Can I link one entry point of the symbol to more pads of the package?**

Assigning one entry point to more than one pins and vice versa is not possible.

**Q6: The problem of associating multiple layout pins to a single schematic entry:**

Associating multiple layout pins to the same symbol entry is not allowed. That means if you have three V+ or V layout pins, you should create three schematic entries for complete assignment. Otherwise you may create SPL0/SPL1 like Supply Pins net for the part. For example you may create SPL\_V+ and SPL\_V by editing the Supply Pins while creating the part. But both these methods are not satisfactory while attaching SPICE models or subcircuits for the part as the subcircuit normally will have only one V+/V node. Now there are two work around methods to solve this problem:

1) Create a symbol with three V+ nodes and three V nodes and complete the part. Now edit the subcircuit file using a text editor to change the number of subcircuit nodes equal to the number of entries of the symbol. You may have to add four more node numbers to the .SUBCKT line for accounting two extra V+/V entries. Care should be taken to ensure that the node numbers added do not conflict with the original node numbers. These newly added nodes should be internally shorted inside the subcircuit. Now this subcircuit may be adapted using Subcircuit Adapter linked with the schematic using EDSpice Symbol Editor or EDSpice Simulator and simulated.

2) The second method is to create a symbol with only single V+ and V nodes and assign the subcircuit straight away. But this results in "Unassigned entries/Entry mismatch " error while creating part. Ignoring this error means that the unassigned layout pins should be explicitly routed or these pins should be added to the V+/V netlist before autorouting. There will be a warning " Symbol Entry missing " while routing the trace/net that may be ignored.

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The former method requires some knowledge about SPICE syntax; results in unconventional schematic but is better suited if the layout of the design has to be produced. The latter is an easier method but extra care should be taken for creating the layout of the design.

**Q7: How can I assign simulation function to the symbol with 68 pins in order to edit it. If we can't assign with the same no. of pins , it implies that we can't edit a new component with no. of pins that is not available in the library?**

You can simulate only those parts that have a simulation primitive available for it. In each new release, we keep adding new simulation primitives so that almost all parts provided in Library will be simulated. These Primitives are functional level descriptions of behavior of the simulated components. Executable code and data of the primitives are placed in the Dynamic Link Library files (\*.DLL) which are found in the Library Directory. With these DLLs we define the input and output pins and these have to be matched with that of the symbol while assigning the simulation function so that the simulator can analyze the behavior of each pin.

If you create an entirely new symbol, you have two options:

If the symbol works like any other symbol for which a simulation primitive is already available, you can assign the same primitive to it. If not, you will have to write the DLL (simulation primitives) for simulating it and then assign it. The DLL primitive source code is written in C programming language. The creation or updation of the primitives requires some knowledge and practice with the C programming language.

**Q8: The display of Packaging information is useful for ICs but is confusing for resistors, capacitors etc. Is there any way to have only the information needed?**

Select Options | Packaging Preferences from System task in the Project Explorer. In the window, check off/on Comp.Name, Comp.Desc and Pinout as per your requirement.

Now you may repack the required components either selecting them individually (Tools | Components Pack/Unpack component with option F2 selected) or in a block (Tools | Block Edit | Unpack/Repack components in block with option F2 selected). These components will be repacked according to the set preferences.


**Q9: How can I avoid duplicating the parts already present in Library, because I draw most of them myself and where can I find information regarding case style encoding?**

You can make a list for a particular library with part full name and keep this as a text file for reference. For creating the list, invoke the List Generator by right clicking on the task, System in the Project Explorer. This text will contain all case styles used in the Library.

**Q10: When I choose a graphic tool a default shape is already placed .How can I change the size and direction?**

After placing the graphic tool on the board you have to stretch that particular item to the required size using the tool 'Stretch Item' from the toolbar. Do remember the zoom size value. If you want to create a graphic item from the scratch with a required size then create the graphic items using the place contact points and then select the particular graphic tool and click on the workspace.

**Q11: How can I find dimensions?**

1. You can view the dimensions of graphic items using the tool  "Create items using text " from the toolbar. In the pop up window you can view the properties of the graphic item selected.
2. Another method for measuring the dimensions of graphic item is by setting the reference point. Switch on Preferences | Ref Point and keep the cursor at any point over the graphic item and then press Shift + P. A reference point gets placed there and that point will be in the coordinate 0,0. Now move the cursor to any point of the graphic item to measure the dimension.

**Q12: I know that the padstack is created for 32 layers but I am not able to create a padstack for 5 layers. Is there any other method?**

There is no method for defining Padstack for 5 layers automatically. But you may proceed in the following way. In Padstack Editor, select New Padstack using wizard and select the tab New/Edit. Type in the name and the required parameters. Click on show layers and select the 5 layers which you intend to use and click Make Padstack. The picture clip shown besides displays the padstack you created.

If necessary use the tools given and edit it manually.

**Q14: I want to replace the DIP24 package of a 74xx154 to the SMD-package SOTxx. Is it possible to replace a package, or is it necessary to create a new part with symbol and linked SOT package?**

Yes, it is possible to replace the package without any problem provided the no. of pins is not lesser than the previous one. This can be done in the following way:

Invoke Library editor, select the part whose package is to be changed and change the package name in the package column and ENTER. Select File | Save Part.

**Q15: How do I create a transformer with multiple secondaries and transformers with a center tap secondary that will work in Mixed Mode simulator and in EDSpice simulator?**

In Mixed Mode simulation, you require a simulation primitive for each category of symbol you wish to simulate; for example, as in your case, Transformer with single Secondary winding, Transformer with 2 Secondary windings, Transformer with center tapped secondary etc. This simulation primitive is attached with the relevant symbol for simulation.

**Q16: Is it possible to create a package, which has through holes, but no pads? (i.e. mounting holes). If so how?**

While creating packages, choose the size of pad equal to the hole size of the padstack, so there is no copper for the pad. Proceed as with any other package and you get a package with a mounting hole, but no copper. If you want a mounting hole as such, just create a package with a single padstack with properties as above.

**Q17: I created a new component, Antycip.Part. I cannot find it in library browser during search. Why? How can I have access to my own library?**

If you have created your own library then first you have to add this particular library in library search sequence in Library Browser module. To include this newly created part file in the Search sequence, select the View | Search Sequence menu from the Library Browser/ Library Explorer and check the corresponding, \*.Part, \*.Symbol, \*.Package files that have to be included in the Search list explicitly.

**Q18: Creating a Symbol using the Library editor. I have some pins in a part, which have no connections. Unless I define them in the Symbol, a mismatch error occurs when I define a part. I would like the no connects to be invisible in the Symbol and though the visibility column in a table in the library/edit Symbol/auto generation process allow this.....but it makes no difference. Do I misunderstand the meaning of visibility here?**

If so, is there any way I can generate a part with no connect pins, which does not show them in the Symbol and avoids errors in the part generator?

This option (visibility) may be used to make pinout text for entries visible in the schematic diagram after packaging so that the pin numbers of the entry points can be seen.

You do not have to create pins in Symbol for NC (No Connection) pins. If there are NC pins in the part, just leave free the corresponding pin in the layout. The system automatically takes it as a NC.

Note: Please make sure that all entries in the Symbol are assigned to one of the layout pin for accurate part creation, and also do not assign more than one schematic entry to a layout pin.

**Q19: I have been struggling to figure out the difference between the Library Browser and Library Explorer, what is their actual difference?**

Library Browser:- This utility is used to browse a Part, Package, Symbol or Padstack according some defined criteria. This can be used to find usage of Symbol, Package etc. The user also have the provision to add types of Parts (View | Register | Part Types). Working of this module is similar to WINDOWS Find. The Parts in the search output list may be loaded to Schematic capture or Layout by "Send to"(from the right click menu) or "Drag-Drop". This module supports Numeric Search (Alphabets in the Part name ignored by the Search e.g. With numeric search enabled and searches for 7400 lists all SN7400, 74HC00, 7400D).

Library Explorer:- Working of this is similar to Windows Explorer conforming to EDA standards. This supports Cut, Copy, Paste etc. Copying one library elements to other by just drag - drop or Copy Paste, creating new library file etc. It can sort library elements according to different criteria (there are 14 default criteria for Part, User can add user-criteria.).

**Q20: In Explorer, I have the option to Edit the part, but its 'grayed out' (disabled). if I try to edit from the Browser, presumably because there is no symbol associated with the part.**

It should be noted that all Part files and associated Symbol and Package files must be included in the Search Sequence for using or editing.

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**Q21: I cannot save to 74TTL.part, nor can I rename, cut, copy or do any editing operations on them.**

Library Files supplied along with the package as well as library elements (parts, symbols and packages) stored in the currently loaded project (PROJECT LIBRARY) are SYSTEM LIBRARIES. The System Libraries CANNOT be Deleted, Renamed, Cut etc. i.e. the user cannot alter the System Libraries. You may however edit a System library Part/ Symbol/ Package but after editing, it cannot be saved to any of the system library files. You may save it to a User Library.

**Q22: How can I edit Part/Symbol/Package in the project?**

or

**When I edit a part and want to update the changes to Project Library, the File | Update to Project Library menu item is disabled.**

You can edit Library objects residing in the Project library from Explorer or Drag Drop into Library editor. The corresponding symbol and Package will be taken automatically. You may save to USER Library if you want, Or you may cancel the Save operation. File | Update to Project Library will update the changes in the Part in the Project Library and the changes will be reflected in the Schematic /Layout Editors.

It is possible only to update to Project Library when a part in the Project library is edited.

**Q23: When I save the part (in the new library) and then try to use it in the Schematic or Layout Editor, the changes seem to have disappeared and the original part appears. As far as I can see, I am saving the part correctly and also calling the correct part from the library browser / Explorer .**

This is because you have not included the newly created library in the Search Sequence. You may do so in the following way. Library Explorer | View | Search Sequence | activate the checkbox to the left of your custom library.

A brief note on the use of search sequence. You have three libraries say 74TTL.PART, BASIC.PART and MyCustomLib.PART having the part 7400 and you prefer to load 7400 from MyCustomLib.PART then you need to put MyCustomLib.PART higher than 74TTL.PART and BASIC.PART in of the Search Sequence. The library has System Libraries supplied with the package and Custom libraries created by you. In case you want to select library elements only from your libraries just uncheck System libraries from the Search Sequence or put your custom libraries higher up in the sequence using the arrow keys provided for the same. If you have 100

Part libraries and you need 10 out of these for the particular project then add these 10 to the Search Sequence, which will increase the Search speed and efficiency.

**Q24: I get the error message "Symbol/Package not found"**

This usually happens if you are using converted databases from EDWin 16 or an EDWin32. Saving the Symbols and Packages to user libraries and subsequently adding them to the Library Search Sequence will solve the problem. Also open Field Editor | Select the library | Right click  
Q25: How do I convert old package to new IPC and JEDEC standard compliant names, egs from DIP14 to DIP14/300?

The Packages with OLD NAMES may be automatically converted using an option available in Field Editor | Select Library | Click in the right pane | Right click | Get EDWin 2000 Convention Package name. This option is not available in the Project Library.

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## EDWin 32 and EDWin XP/2000 libraries

### **Q26: Why do I need to use separate copies of libraries and databases/projects for EDWin 32 and EDWin 2000 if all libraries are upward compatible?**

Any attempt (even for browsing using Library Explorer or Browser) to access EDWin 32 libraries from EDWin XP/2000 environment causes permanent change of format of EDWin 32 libraries. EDWin 32 libraries and databases once used with EDWin XP/2000 cannot be used with EDWin32. Therefore it is imperative to use separate copies of libraries and databases for EDWin 32 and EDWin XP/2000.

### **Q27: How do I add a new manufacturer?**

Library Browser | View | Register | Part Types | Select the Manufacturer Tab | Right click on any of the entries | Add Top Level. Similarly new Type / Technology and Package type can be added.

### **Q28: I need to create components with oval holes, I mean I need not only OVAL padstack, the component pins are not cylindrical but are a small slabs so I need a way to define a slot in the center of the padstack. Can you give some hints or ideas about how to define this kind of holes in order to PCB manufacturing firm can understand my Gerber and Drill files?**

1. Create an Oval (Name:Oval) Padstack (using Padstack Editor) with the desired width (more than the width of slab pin). This padstack should have a hole diameter just greater than the thickness of the pin.



2. Create another Empty (Name:Empty) padstack (using Padstack Editor) with hole diameter equal to the hole diameter of above padstack.

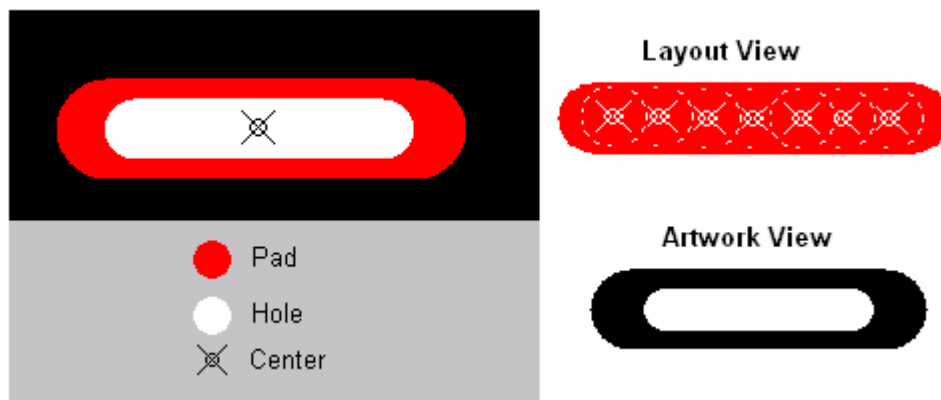


3. Create a New Package (using Package Editor) and replace the default pad #1 with the Oval Padstack.

4. Then place and repeat the Empty padstack in both sides of the hole of above (Oval) padstack. Adjust Grid and Snap properly in order to repeat and place the padstacks.



After placing necessary Empty padstacks, save the package and using this package create a Special Part. Save this part in the required library.



Observe the above figure , it shows the layout and artwork view of the created part.

## Simulation

### Mixed Mode Simulation :

**Q1: Let's say that I had created 16 input XOR, 16XOR, and I assign it with simulation function of 2XOR. Now will the function of the component be as the XOR one?**

In order to simulate a 16 XOR with 2XOR, you will have to write the truth table and create a circuit that produces the same functionality as 16XOR using 2XORs (or any other simulated gates). In EDSpice you can attach this subcircuit to 16XOR. In this case when you run simulation, the Simulator will take the simulation results of the subcircuit attached to 16XOR. However attaching subcircuits is not possible in Mixed Mode Simulator. In Mixed Mode, you will have to replace 16XOR with the corresponding reduced circuit and then run the simulation.

**Q2: Provision is made only for entering the text in the 'Schematic Editor' and if I enter the component values as text then they do not change when I change the value of the component during simulation.**

The value may be given to the component using Add/ Change Text tool along with the option, Add/ Change value enabled. This value is accepted by Simulator. But after every change is made, remember to run Preprocess in Mixed Mode Simulator window to make the changes active.

**Q3: I can't simulate a Logic Component like Operational Amplifier or Multiplier (AD632). In fact, when I go to Mixed Mode Simulator, it says that it's a not simulated component. But in Database filter, there is no problem. Do you have an answer?**

To know whether a component can be simulated or not, open Library Browser. From View | Options menu, check the option 'Simulation Function' and search for the component. If the component is having a simulation function, the information will be listed in the table corresponding to 'Simulation Function' below after the search.

AD632 does not have simulation functions assigned to it. The only OPAMP that has simulation primitives assigned to it in mixed mode is OPAMPA in the library file a\_linop.SYMBOL. The same simulation primitives may be assigned to any other opamp that has matching number of pins.

**Q4: How can LED's and 7 segment displays be simulated?**

You can assign the simulation function for Diode to LED symbol and do the simulation in Mixed Mode Simulator. In EDSpice, there are Model parameters for LED's in LED.sparam.

**Q5: What is written in clock generator string to output 15 KHz clock pulses? How can 15KHz clock pulses be detected?**

(H20,L47)[us] as generator string, will produce a Pulse train, starting with a Mark of 20 micro seconds and a Space of 47 micro seconds, the time period is 67 micro seconds (for 15KHz, it is 66.67 micro seconds, To increase the precision, choose time in nano seconds, ns instead of us, and give appropriate values). For a pulse Train of 100, the generator string is 100(H20,L47)[us]. Add '

Logic state TP' right at the pin where you assigned the Generator String and when Transient analysis is done, you get the Pulse Waveform in the diagram.

**Q6: Can custom Mixed-Mode simulator models be created?**

Yes, custom mixed mode simulator models may be created provided simulation primitives are available. If the symbol works like any other symbol for which a simulation primitive is already available, you can assign the same primitive to it. If not, you will have to write the DLL (simulation primitives) for simulating it and then assign it. The DLL primitive source code is written in C programming language. The creation or updation of the primitives requires some knowledge and practice with the C programming language. You may find the necessary documents for this on the CDROM under the directory named Sim model.kit.

**Q7: I'm trying to add a new component to the library and have some questions. When creating a new Part, you can assign a simulation function to it. But I can't find the way of specifying it's electrical characteristics and save them within the Part. Where can I enter these parameters?**

You can assign simulation function to a symbol. After assigning the simulation function to the symbol, load it into the project. Invoke Mixed mode Simulator and select the tool "Set parameter" (option tool of the functional tool "Set parameter/ Models") in the tool bar and click on the symbol. You will get a window where you can edit/ enter the values. Save the edited parameters into a separate library.

**Q8: Making changes to schematic circuit and preprocessing does not appear to re-configure the 'nets' correctly i.e., have to re-edit the nets?**

Always see that you edit the net and not the wire connection. For example if you delete a wire in schematic, the wire gets deleted but the net remains. So after preprocessing, the net still remains. Before making any changes to nets you should confirm that you deleted the net or a part of it. Deleting wire connection will not delete net connection. It only deletes physical representation.

**Q9: I am trying to use the mixed mode simulator to calculate power on a resistor. In the waveform viewer, I click ADD to add a trace, then type in a formula PWR (R9) that generates an error when I try to APPLY it. The plot shows zero power. How do you get a plot of the power in a resistor?**

To calculate the power in a resistor, you should place two markers for voltage and current at the resistor node and from the equation generator, explicitly enter the variables in the format Voltage\* Current and then calculate the power.

For e.g.: enter in the expression list box:

V1 (GEN) \* I1 (Unpck16: PIN1)

to calculate the power at a resistor. And in the Units list box enter the unit to which the diagram should be displayed, i.e. W.

The PWR function is unused for calculate the X raised to the power of Y.

For e.g.: PWR (3,2) which will give you 9 as output.

**Q10: How do I simulate my assembly language program ( 8051) in the Simulator?**

The library has a primitive for 8051 microcontroller, therefore it will be possible to simulate it if there is an associated binary file of the Assembly language program. The binary file may be assigned to the microcontroller as follows: Mixed Mode simulator | First function tool "Set Parameters / Models" | First Option tool "Set Parameter", click on 8051 and a window titled "Component Parameter Setup" appears. Click on "Setup" | "Load Binary file" | Browse the path to the Binary file. Click on "Disassembler" to verify the Assembly code. How to create the binary file is explained in Help files. (Mixed Mode Simulator | Help | Notes on "How to simulate 8051 circuits").

## EDSpice Simulator

**Q1: Where can I change the limits of the simulation if the error 'Iteration limit reached' appears?**

You can change the Iteration limit by selecting Analysis | Simulation Variables (Options). This pops a list of simulator variables that maybe set. Click on the option 'Reset DC Iteration Limit' and enter the new value.

**Q2: A problem I have encountered is that when I use the spice netlist generator, from inside the EDSpice simulator, in order to run the simulation with another Spice engine or just to check it, all nodes have different numbers than that of the schematic and the original Spice circuit.**

EDSpice uses node numbers (EDSpice Node Id) for internal manipulation. The program for internal use creates this. However, net names that you have given in Schematic are retained in EDSpice. You can view this using the tool Component Info.

**Q3: What is Gmin Stepping error? I am lack of information, examples and about the errors that occurs in EDSpice.**

GMIN stepping Error

GMIN stepping is EDSpice's default DC convergence algorithm. "GMIN stepping failed " error message means that due to some reason, the Simulator is unable to solve the given circuit. Some probable reasons are following:

1) The elements in the circuit might have not set up properly. Check all symbols in the circuit and ensure that all of them are properly set up, and appropriate models are defined wherever needed.

2) Another common reason is the absence of DC path to ground at some analog node. This may happen while cascading capacitors, inductors or code models. For such situations select "RSHUNT" option (Setup - Simulator Variables (Options)- Shunt Resistance from analog nodes to ground RSHUNT =) and enter 1T. This automatically introduces 1 tera ohm resistance to ground at all analog nodes in the circuit to help it to converge.

3) Another reason is a loop of voltage sources and/or inductors or a series connection of current sources and/or capacitors. To get around in such situations, use a very small resistance in series with inductors, or a very large resistance in parallel with capacitors.

In the Help pull down menu in the EDSpice Simulator module, you have a topic How to use EDSpice. Selecting this, you will get the EDSpice Interactive Module Help file. This Help file should give you all the information you require on EDSpice. Click on the last topic EDSpice Example projects and go through the examples.

#### About Errors in EDSpice

The documentation of errors that occur in EDSpice is available. After invoking EDSpice Simulator, select EDSpice Reference under the Help menu item. In the Contents of EDSpice Reference Help, you have a topic 'Error Messages '. Go through this for explanation of errors that may be encountered while attempting to run a simulation.

#### **Q4: Does EDSpice accept a SPICE Library in ASCII format?**

EDSpice does accept model parameters and subcircuits in ASCII format. As EDSpice provides a graphical environment, slight modifications are to be made to these library files. To do this, library files may be adapted to the form accepted by Spice. In order to adapt to EDSpice Libraries, they should be compatible with the SPICE 3F5/XSPICE format. The adaptation of the ASCII libraries may be done as given below:

To adapt model parameters:

Select Project Explorer. Right click on the task System and select Model Parameter Editor. Select File | Extract from Netlist from the window that pops up. This allows extracting details from the file. The parameter may be saved in a .Sparam file.

To adapt subcircuits:

Select Project Explorer. Right click on the task System and select Subcircuit Adapter. From the window that pops up select File | Open. This allows extracting details from the selected file. The subcircuit may be saved to a .sbc file. For more details, refer help files.

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**Q5: Is EDSpice capable of doing audio frequency spectrum analysis a (Bode Plot) of a state variable bandpass filter?**

EDSpice is capable of doing audio frequency spectrum analysis. However it will not generate the Bode Diagram. You can run Pole Zero Analysis in EDSpice and get a textual output.

**Q6: Why and how Pole-Zero analysis?**

Pole- Zero analysis is mainly done to find the stability of a system. If a pole exits with a positive real part, this will result in a disturbance increasing exponentially with time. Hence the condition which must be satisfied, if a system is to be stable, is that the poles of the transfer function must all lie in the left-hand half of the complex-frequency plane.

Consider the case of an amplifier with negative feed back and without feedback. Pole-Zero analysis gives the result with lesser pole values (negative) for amplifier with feed back than the pole values for amplifiers without feedback indicating that the amplifier with feedback is more stable and thereby having more frequency response.

In EDSpice before Pole-Zero analysis the corresponding nodes are to be set. NODE1 and NODE2 are the two input nodes and NODE3 and NODE4 are the two out-put nodes

CUR stands for a transfer function of the type (output voltage)/(input current) while VOL stands for a transfer function of the type (output voltage)/(input voltage). POL stands for pole analysis only, ZER for zero analysis only and PZ for both. This feature is provided mainly because if there is a non-convergence in finding poles or zeros, then, at least the other can be found. Thus, there is complete freedom regarding the output and input ports and the type of transfer function.

**Q7: Can you advise me on the correct usage of the EDSpice adder and multiplier blocks?**

The adder (summer) is a block with 2-to N input ports. Individual gains and offsets can be applied to each inputs and outputs. Each inputs is added to its respective offset and then multiplied by its gain. The results are then summed, multiplied by the output gain and added to the output offset. This model will operate in DC, AC, and Transient analysis modes.

The multiplier is a block with 2- to N input ports. Individual gains and offsets can be applied to each inputs and outputs. Each inputs is added to its respective offset and then multiplied by its gain. The results are multiplied along with the output gain and are added to the output offset. This model will operate in DC, AC and Transient analysis modes. However, in AC analysis it is important to remember that results are invalid unless only ONE INPUT of the multiplier is connected to a node, which bears an AC signal.

**Q8: What extra features does EDSpice simulator offer?**

It provides different types of analysis according to your circuit design.

In addition to its analog simulation capabilities, EDSpice also allows efficient simulation of mixed-signal (analog/digital) circuits and systems. It completely buffers the user from the SPICE netlist through easy-to-use dialog windows. A unique feature allows the extraction of SPICE.MODEL lines and Subcircuits, from existing netlists, to be saved in special libraries. They can then be reloaded or edited later on. Hierarchical schematic diagrams are directly translated into SPICE netlist syntax. This means the hierarchy structure is maintained by using Subcircuits. Simulation results can be viewed in standard SPICE2 format or plotted as graphs in Waveform Viewer.

**Q9: In EDSpice, is it possible to force in the inputs any type of multishape signal defined by the user, similar function to VPWL\_FILE of MICROSIM?**

Yes, in EDSpice we can attach PWL files to the source. For this you have to select the tool "Set Parameters Models" and click on the source symbol to get the Instance parameter window. Click on the row for instance parameter named "Source function"(last one) to get the "Source function" select window. This parameter will be available only for components, which act as source. Select PWL from the list and this will display the function parameters in the list provided. Either you can edit the parameters there itself or you can load already created PWL file using the button "LOAD VALUES FROM FILE". "Repeat items" edit box allows to enter the number of times you want to repeat the function parameters for the file.

**Q10: Can we load from Internet, a Spice model of component from any manufacturer (Texas...etc..) then use it in EDSPICE?**

Yes, you can do this using Subcircuit adapter.

To adapt subcircuits -

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- 1) Select Project Explorer. Right click on the task System and select Subcircuits Adapter. From the window that pops up select File | Open. This allows extracting details from the file.
- 2) The display window will list the selected SPICE netlist.
- 3) The subcircuit should start with a .SUBCKT line and should end with .ENDS line. Before using a subcircuit for simulating with EDSpice, you should adapt it using Subcircuit Adapter and attach it the symbol.
- 4) The subcircuit adapter receives information about the nodes and stores it in the beginning of the subcircuit file as SPICE comments (lines starting with \*). This information is used to graphically attach the subcircuit to the part. It is must to supply a description for the subcircuit including one for each of the available nodes. The description for each node is typed into the edit box called "Description" and is accepted by pressing the ENTER key on your keyboard. The column "Node Type" allows to select the node type of the subcircuit.
- 5) The adapted subcircuit is saved into a proper sub-directory under ..\EDS\_SBK. Before adapting the subcircuit, make sure that the Subcircuit file name and the name of the subcircuit mentioned in the .SUBCKT line are the same. This will avoid unnecessary warnings while pre-processing. Subcircuit name can have eight characters.

**Q11: How do I simulate 8051 (Assembly language program) with EDSpice?**

First Function tool "Set parameters / models" | Click on 8051 | Click on "Set up Model!" | Input file – click on "Not set " | Select the \*.bin file which is the binary file of the Assembly language program.

For more information on how to create a binary file please refer Mixed Mode simulator | Help | Notes on "How to simulate 8051 circuits".

## PCB Analyzers

### **Q1: Steps to generate Thermal effect on the board**

To display thermal effect on the board, follow the steps shown below.

1. Set the colors using the tool “Display Parameters” which is helpful in displaying a colored board. Each color represents a range of temperatures. To set the color, click on the color corresponding to a particular temperature to pop up a color palette. Select the required color.
2. Now click “Execute” tool. This displays the Isotherms indicating the thermal effect on the board. The various temperature on the board may be labeled using the tool Set/ Delete label.
3. To display the temperature distribution on the board, select Thermal/ Colored board from the drop down of View menu. The status bar at the bottom of the window shows the temperature at the point where the cursor is positioned.

### **Q2: Steps to generate Electromagnetic field intensity on the board.**

To display field effect on the board, follow the steps shown below.

1. Select Electrical parameters tool, which pops up a dialog box. Add the nets and assign the voltage and frequency values.
2. Set the colors using the tool “Display Parameters”. This tool allows to map a set of colors to a set of field intensity in order that after analysis the electromagnetic field intensity may be visually displayed on the screen. To set the color, click on the color corresponding to a particular field intensity to pop up a color palette. Select the required color.
3. Now click “Execute Analysis” tool. This displays the Isolines indicating the field intensity on the board. The fields intensity on the board may be labeled using the tool Set/ Delete labels.
4. To display the field intensity on the board, select EMA Display/ Colored board from the drop down of View menu. The status bar at the bottom of the window shows the field at the point where the cursor is positioned.