
New features from EDWinXP ver 1.20 to EDWinXP 1.50 – DETAILED

i) New Features of EDWinXP 1.20– What's New

Common Features

1. Physical and Logical view:

EDWin Interface has been devised in a new way such that it is made more user friendly. The expandable/ collapsible hierarchy of folders present in EDWin Project Explorer now appears colorful to distinguish between different functional operations.

The EDWin Project Explorer is now divided into two tabs, one is Physical view and the other is Logical view. These types of view are significant when working with hierarchies. Logical view shows the relationship between the circuit hierarchy, whereas physical view just displays the circuit hierarchy.

2. Project Tasks:

New tasks are now included in the Project Explorer to do the following operations with considerable ease.

Add circuit: Allows to give a name to the new circuit added to the existing project. This circuit can have a relationship with other circuits.

Load circuit: Allows to select already existing circuits to the current project.

3. Circuit Tasks:

New tasks are now included in the Circuit to perform the following operations with considerable ease.

Rename circuit: Allows to rename the selected circuit.

Save circuit: Allows to save the selected circuit file.

Delete: Allows to delete the selected circuit.

4. Inserting new values for Text sizes and Line sizes in Options setup:

For both schematic and Layout, user can insert the desired new value while removing an already existing unwanted value. The list will be automatically sorted in ascending order and the new value will be placed in the corresponding position.

5. Some of the main editors like Schematic, Layout, Library may now be invoked by double clicking on the task in the Project Explorer.

6. In earlier versions, a project file could be opened by using the menu items present in the Project Explorer. But in this version of EDWin, a project file may also be opened by drag and drop from Windows Explorer into the EDWin Project Explorer.

7. Normally, library elements are shipped along with the Installation CD. These elements are automatically installed during installation of the package. With this release, around 25,773 library parts, 729 mixed mode primitives and 886 spice models are packed with the installation CD.

8. Locking of dockable toolbars:

The new version of EDWin XP is provided with a unique feature to lock the dockable toolbars anywhere within the window. Select the menu Preferences/ Lock Toolbar or use shortcut key (CTRL+H) to lock / unlock the toolbars at that particular position.

9. All the icons are made transparent throughout the modules.

10. Export/ Import Utilities:

In addition to the already existing Export/ Import Utilities, four new export and two import facilities have been included with this release.

Ø EXPORT formats:

1. EDWin Schematic Netlist
2. Xilinx Netlist.
3. CUPL Netlist.
4. JEDEC Netlist.

Ø IMPORT formats:

1. EDWin Schematic Netlist
2. VHDL

Also three converters have been included to convert EDWin Schematic Netlist to CUPL, XILINX or JEDEC Netlist.

11. VHDL:

This version of EDWinXP helps to describe the behavior of digital systems with the help of VHDL. VHDL is a programming language, using which the logic involved in the working of any digital circuit may be written to generate models for simulation. These models may then be used as basic building blocks in larger circuits. VHDL Editor has been included for writing VHDL programs.

12. Simulation Model Generators:

The model generators allow converting VHDL source files to models for simulation purposes. Since EDWinXP supports two forms of simulation – Mixed Mode and EDSpice, two model generators have been included – MM Simulation Model Generator and EDSpice Simulation Model Generator.

Schematic Editor**1. New Option tools:**

In Tools->Components->Hierarchy down->

Ø Set subcircuit I/O nodes: Allows to assign input/output nodes of the subcircuit.

Ø Check assignment of subcircuit I/O nodes: Allows to check or re-assign I/O nodes.

In Tools->Components->Repeat Component->

Ø Copy Component Value: Allows to copy the value of a component while replicating the component.

In Tools->Block Edit->Copy Block->

Ø Merge Pwr/Gnd Net: Merging of only the Pwr/Gnd nets is made possible while copying components using Copy Block function, Shift key or Bulleting.

Ø Copy Component Value: Option to copy a block of components along with their assigned values.

In Tools->Block Edit->Load Block->

Ø Merge Pwr/Gnd Net: Option for merging only the Pwr/Gnd nets while loading the block to project.

Ø Copy Component Value: This option tool can be used to load a block of components along with their assigned values.

Note: Turn ON this option while using shortcut keys or right click menus for copying and loading components in order to load the component values also.

2. Revised Function Tool:

Q Autoplacer:

The new autoplacer is a sophisticated tool, which does the function of placing all components on to the page and is interactive and flexible. There is no predefined procedure or sequence of operations but certain convention must be observed.

- a) Only components located outside of the page (present in the bins) are selected for placement. Components, which are currently located on the page, are considered as "already placed".
- b) Only the components with at least one net connected pad are selected for placement. Totally disconnected components are ignored and have to be placed manually since it cannot be predicted which position on the page is optimal for unconnected components.

Autoplacer can perform the following operations:

- a) It can automatically place all components outside of the page boundaries and sort them according to parts.
- b) It allows user to relocate single components and manually place them according to selected placement cell patterns.
- c) It allows user to identify other components connected to selected component on the page and manually place them according to selected placement cell patterns.
- d) It allows to automatically place components connected to a selected one.
- e) It allows to automatically place all connected components starting with those connected to a selected component.
- f) It allows building groups of components and relocating these groups to desired position on the page.
- g) It allows automatically building new groups of components using the currently present group as template and relocating this newly created group to desired position on the page.

3. Removed from 1.20

Certain functions are replaced with sophisticated ideas and therefore the following old tools and functions are now totally removed to fit in new features.

∅ Relocate by pattern: Since autoplacer feature is completely revamped, this tool is no more required. So this tool has been removed from Component->Relocate component tool.

∅ Autorouter functions: Autorouter functions are now incorporated in Wires & Buses tool bar. So the separate set of tools present in earlier versions is now completely removed. Also menu items present under Preferences menu of Schematic Editor like AutoRoute to pin connections and Reroute component connection after move facilitate automatic routing to some extent.

∅ Keep off zones: Keep off zones tool sets are removed because now keep off zone is now split into two categories like Placer keep off zones and Router Keep off zones. These two tools are now kept in Layout Editor.

∅ Placement pattern: As the autoplacer is revised with a completely different idea, the old set of tools is removed.

4. Creating and Loading strategies for Semi autorouting:

While using Tools->Wires->Route Wire->Autoconnect Wires, it is possible to define a routing strategy including routing schemes, autoconnect rules and routing options like Font Name, Font Size, Minimal Pin Size etc. and can be saved as a Schematic Strategy File (*.SSF) within the Lib folder. These saved strategies can be further loaded in a project for routing.

5. Remembering Preset Values:

∅ Remembering T-connections ON/OFF:

Each time Schematic Editor is opened, the system keeps the option tool Allow T-connections either ON/OFF depending on the previous status of this tool.

∅ Remembering setting of Scroll bar:

Each time Schematic Editor is opened, the system remembers whether scroll bar was ON/OFF in the previous instance.

∅ Remembering Preference menu settings:

The last set value for the menu items Preferences-> Zoom Factor and Preferences -> Reroute component connections after move are also retained between subsequent opening of Schematic Editor.

Layout Editor

1. New Option tools:

In Tools->Components-> Open Part Library->

∅ Add Test points with Through hole: Allows to place a test point with through hole on a trace in any layer. Component nodes can also act as a test point, which may be placed on any layer.

∅ Add Test points on Surface Layer: Allows to place a Test point, which is a single pad component and may be placed on the top and bottom layers only.

In Tools->Components->On/Off Component Name->

All component names can be switched On/Off at a time using the two new option tools:

Ø On All Component Names: Option to display all component names on the board.

Note: The component names are displayed in the default font size set in the Options setup.

Ø Off All Component Names: Option to switch off all component names on the board.

In Tools->Traces->Route Trace->

Ø Toggle Arc Insert: Option to draw smooth curved traces.

In Tools->Block Edit->Copy Block

Ø Merge Pwr/Gnd Net: Option for merging of only the Pwr/Gnd nets while copying components using Copy Block function, Shift key or Bulleting.

In Tools->Block Edit->Load Block

Ø Merge Pwr/Gnd Net: The option is made available for merging only the Pwr/Gnd nets while loading the block to project.

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q Board Outline

There are new and improved tools for defining the board outline. Board outline may be defined in any of the following methods.

Defining Board outline from the Layout Editor:

- i. Using Contact points.
- ii. Polygon draw Method
- iii. Create Board Outline Textually

Defining Board outline from the Fabrication Manager:

- i. Import Board outline from the artwork of an existing PCB
- ii. DXF board outline Import:

Board Outline also has option tools for creating cutouts, regions, templates, placer keep off zones and router keep off zones.

Cutouts: Cutouts are areas on the board that is useful for mechanical purposes. They may be defined in different shapes according to the requirement. Cutouts are placed using the tools available in Tools-> Board Outline.

Regions: Regions are areas defined on the board where specific DRC rules may be set and applied. Regions are placed using the tools available in Tools-> Board Outline.

Templates: Templates are areas defined on the board where specific components may be tagged to, so that only the tagged components are placed in the defined templates while autoplacing. Templates are placed using the tools available in Tools->Board Outline.

Placer keep off zones: They are usually defined on the board to restrict the autoplacer from automatically placing the components in the defined area. Placer Keep-Off-Zones are placed using the tools available in Tools-> Board Outline. Autoplacer is prevented from using the Router Keep-Off-Zones area for routing purposes.

Router keep off zones: They are usually defined on the board to disallow the autorouter from automatically routing the component connections in the defined area. Router Keep-Off-Zones are placed using the tools available in Tools-> Board Outline. Autorouter is prevented from using the Router Keep-Off-Zones area for routing purposes.

3. Identification of Selected pin in Layout through property window:

Select the function tool Component Property and click on a component pin to get the component property window with the selected pin highlighted in the left pane.

4. Remembering the last set value for the menu Preferences-> Zoom Factor.

5. Removed from 1.20

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Ø Relocate by pattern: Since now autoplacer feature is completely revamped, this tool is no more required. So this tool has been removed from Component-> Relocate component tool.

Ø Keep off zones: Keep off zones tool sets are removed because now keep off zone is now split into two categories like Placer keep off zones and Router Keep off zones. These two tools are now kept in Layout Editor.

Ø Placement pattern: As the autoplacer is modified with a completely different idea, the old set of tools is removed.

6. Layout DXF Export:

The graphical interface of Layout DXF Export has been changed to make it more user friendly. It also provides facility to export 3D information of the board and its contents.

7. 3 Dimension:

With this version of EDWinXP comes the most exciting concept of 3-dimensional view of electronic circuits in design stage itself. You can get a real life view of the designed board from

different angles and directions. You can also detect the path taken by a trace much more easily with this facility.

Library Editor

1. Saving the settings:

Various settings in Symbol Editor, Package Editor and Padstack Editor such as Zoom Factor, Enable Undo and Redo and the different tool bar views can be saved with the system. For this to take effect, after making the necessary changes in a particular editor, the user needs to switch between tabs to save these changes.

2.The special character "%" can be used within a Part name. For example, a Part can be named as 100K20% to represent a 100-kilo ohm resistor with a tolerance of 20%.

3. 3-Dimension:

The concept of 3-Dimension has been incorporated in Library Editor for package creation. Now all library elements in EDWinXP are available with 3-D information. A new editor named Board Cabinet Editor has also been added to get 3D view of boards arranged in cabinets of various shapes.

4. Default addition of library files to search sequence

The newly created library files (.part,*.symbol,*.package,*.padstack) can be included to the topmost position of search sequence.

Library Explorer

1. Remembering settings in the preview:

The system remembers the previous settings such as true size, pad frames etc. of the Symbol/Package preview window each time the window is invoked using the menu View->Preview.

2.The shortcut key F2 can be used to rename a custom Part.

Fabrication Output Manager

1. Graphic Import and Reconstruction of graphics (Reverse Engineering):

This feature is an enhanced version of the earlier Graphic Import Editor that was available with EDWin 16. For EDWinXP users, this feature is a boon as Reverse engineering was not possible with EDWin 32 and EDWinXP/2000.

The function of this feature is to import/ reconstruct (reverse engineering process) a PCB from the final outputs generated using EDWin or other E-CAD/ CAD softwares. As of now, EDWin is prepared to handle *.GBR, *.DXF files and user is supposed to convert these to intermediary format *.ART files. These *.ART files are imported and the layer contents in the artwork file are assigned to specific masters or categories. Finally, using the Reconstruction tool each object is reconstructed individually in order to reconstruct complete or selected parts of Project Database.

2.DXF Preprocessor:

DXF files are ASCII information of graphical primitives done in AutoCAD. These files may be converted to artwork files, which may be processed in EDWinXP to get back the gerber files. Using this provision user may import DXF files for the following purposes.

- a) Complicated board outlines with or without cutouts done in AutoCAD. Resulting graphics can be imported to EDWin and used to reconstruct same PCB outline in the Project Database.
- b) Placement markings for aligning Components.
- c) Complicated geometric shape for copper pour.

3. Export in GenCAM format: This is a special format generated, which is accepted by photoplotter other than Gerber.

4. The tool magazine size of NC-Drill is increased from 32 Tools to 500 Tools.

5.Setting Offset:

While viewing the artwork files in Gerber Preprocessor and Viewer dialog, if the artworks of various layers are not aligned properly, they can be adjusted by setting the X & Y offset values.

Mixed Mode Simulator

1.New Option tools in Hierarchy down->

Ø Assigning subcircuit I/O nodes: Allows to assign Input/ Output nodes of the subcircuit. Whenever a subcircuit stored in the Library is associated with a symbol, its input and output nodes must be assigned to appropriate entries. The functions of these nodes depend on the way they are connected within the subcircuit. For example, if a subcircuit executes the logic function of

a two input NAND gate, it is necessary to define the input nodes and the output node. The sequence of nodes is irrelevant as long as they are properly assigned to the entries of the symbol, which is linked to this subcircuit.

Ø Check/ Edit the assignment of subcircuit I/O nodes: Allows to check/ re-assign I/O nodes.

2.New Function Tool

Ø Net Info: Allows to highlight the selected net.

3.Revised Feature:

Oscillograph: The Oscillograph is enhanced and is made interactive with the simulator. Now net names are displayed on the output oscillograph window and new waves may be added. The settings that are made in the Oscilloscope are made available till the module is closed.

4.Record Simulation Output in Oscillograph as PWL file:

In previous versions Signal Integrity was analyzed by giving arbitrary waveforms (like Square Pulse, Sine, GND etc). It is now possible to give the test input conditions (which is normally given in the simulator) in Signal Integrity Analyzer, which gives the advantage of simulating the actual conditions.

The output values obtained during simulation in oscillograph can be recorded and saved in PWL file.

5.Transfer Function Analysis:

Now it is possible to enable/disable Transfer Function Analysis while setting parameters for Transient Analysis.

EDSpice Simulator

6.New Option Tool for Net Info->

Ø Highlight TP net/ node: Allows to display the nets or pins to which a given test point is assigned.

7.Revised Feature:

Oscillograph: The Oscillograph is included in EDSpice with this version of EDWin. It includes all features that Mixed Mode Oscillograph offers. Oscillograph is enhanced and is made interactive with the simulator. Now net names are displayed on the output oscillograph window and new waves may be added. The settings that are made in the Oscilloscope are made available till the module is closed.

Waveform Viewer

1.New items in File menu:

∅ Save All : This option allows to save multiple waveforms simultaneously to the Job folder. The waveforms are identified by default names which include the date and time of creation.

∅ Save All to Project : Multiple waveforms can be saved simultaneously to the current project by using this option. The waveforms are identified by default names which include the date and time of creation.

ii) New Features of EDWinXP 1.30 and EDWinXP 1.40 clubbed together – What's New**Schematic Editor**

1.New Autoplacer tools:

In Tools | Autoplace

∅ Group by category: This function tool along with a set of option tools may be used to group components together in the bins based on certain criteria like nature of, nature of connections or nature of terminals.

Option Tools include:

Include already placed: Option to include already placed components in the category group.

Group 'Input' components: Groups components which are connected to input nets for the page. The components with single nodes on the left side are detected by the autoplacer as input nets.

Group 'Output' components: Groups components, which are connected, to output nets for the page. The components with single nodes on the right side are detected by the autoplacer as output nets.

Group by bus: Groups components connected to a bus and places them in the Component Groups Bin.

Group by net: Groups components connected to a net and places them in the Component Groups Bin.

Group 'Input' terminals: Option to group components recognized as 'input-to-page' terminals.

Group 'Output' terminals: Option to group components recognized as 'output-from-page' terminals.

Group 'Inside' components: Option to group all the components, which are not included in the input or output category.

Append group: Enables groups of different categories to be accommodated in the Component Groups Bin at the same time.

∅ Relocate Component: Tool to relocate component/ component text. Options may be used to rotate by 90°, any angle, change the placement side, relocate component with name specified, swap components placement, toggle display of ratsnest/ trace/ outline etc.

∅ Relocate Block: Tool to relocate selected block to another position. Its set of options may be used to rotate the block by 90°, any angle, and to relocate items in the block including the page outline.

∅ Reroute Connections: Tool to autoroute wires while carrying out Manual / Autoplacement. This tool has been provided for convenience so that the user does not have to take the trouble of switching to Tools | Wires & Buses to start routing the connections.

∅ Net Property and Component Property: Tool to view/change properties of selected net and/or component.

In Tools | Autoplace | Autoplace all components

∅ Autoplace Topologically: Option tool to place components automatically based on circuit topology.

2. Instant Packaging

This new menu item under Preferences menu in Schematic Editor helps to pack components as soon as they are loaded to the workspace. All the constituent groups of the part will be loaded. This is particularly useful while loading connectors into the Schematic.

3. Autocovering

Auto covering avoids switching between the tools. Option tools delete, properties and relocate are now common in all the function tools. In order to avoid confusion between nets and traces a common tool named connections is introduced in which the nodes option has also been included.

4. Component Browser

Customizable component browser has been introduced in Schematic Editor. The browser embedded in Schematic Editor provides the facility to browse and search for components.

5. Block Diagram Elements

This feature allows for simplified creation of block diagrams of hierarchical circuits. There is no longer need to create block diagram elements using Library Editor since part descriptions

and symbols are automatically created according to user's specification. Nevertheless, parts and symbols created for block diagram elements may be edited like any other library element and stored in the disk libraries for farther use.

6. Component Specific MM Simulator Models

Mixed Mode simulation models may be assigned individually to components, hence overriding current model assignment to symbols. Component specific simulation models may be assigned to block diagram elements.

7. Truth Table to diagram converter

Logic function defined in form of truth tables may be converted to equivalent schematic diagram that may be later attached to currently edited page, form a new page in edited circuit or be attached as new circuit in the project.

8. Direct assignment of logic function to schematic components

Logic function of selected schematic component may be specified either through truth table or VHDL code and attached in form of hierarchical sub-circuit or automatically generated simulation model. Generation of both MM Simulator and EDSpice code models is supported.

9. VHDL Code Converter

This function enables conversion of VHDL code into schematic diagram.

10. Vertically or horizontally oriented net/bus page link notes

Depending on user's preference, net/bus page link notes may be generated either as vertical or horizontal bar. Vertical bar was the only option in previous versions.

Mixed Mode Simulator & EDSpice Simulator

1. Model Interface

Model Interface is a centralized management tool, used for configuration of any kind of either analog or digital component of Mixed-mode Simulator. It allows the simultaneous administration of different components on the model level.

2. Transient Analysis - Logic Analyzer:

Now it is possible to directly launch the Logic Analyzer from the simulator window. A user may use this dialog to get the textual values for digital (binary, octal, hexadecimal and decimal) and analog waveforms at different test points.

3. Multichannel display in Oscillograph:

Option to view four channels in their respective axes simultaneously.

4. EDSpice Interactive Interpreter:

EDSpice Interactive Interpreter has been revamped to include features to directly initiate simulation from .cir file. Apart from this, it also incorporates features for creating new, editing and saving existing .cir files.

5. Simulators embedded in Schematic Editor

Both Mixed Mode and EDSpice Simulators are now incorporated in Schematic Editor, thus avoiding the need to switch between the modules.

6. Circuit File Editor

Circuit File Editor is used for editing SPICE circuit file and running simulation. The circuit file (.CIR file) describes the circuitry to be analyzed in a format that the SPICE simulation engine can interpret.

7. Instant Probes

These probes are used for instant display of transient analysis result of desired nets/nodes in an analog/digital circuit.

8. 8051 Microcontroller Kit

The kit contains new simulation model of microcontrollers of 8051 family and application examples. The 8051 model uses MMI technology that enables edition and compilation of programs in C-language and assembler, debugging the code and simulation together with whole circuit. Attached simulation examples help in evaluating the kit and learning how to use the model for the development of microcontroller programs. The kit contains also series of so called instrumental model for generating parallel and serial binary data patterns and asynchronous hardware interrupts. Usage of 8051 model in user's designs requires separate license.

This kit includes example project databases designed to illustrate functionality of the new simulation model for 8051 microcontrollers. Each project comes with associated help file that explains the example in details.

The latest software version of the model is included as well as 8051 code C compiler and function libraries. The new MMI model for 8051 allows coding programs in C or Assembler and debugging them in real time while functioning of the rest of circuitry is simulated.

To facilitate analysis of more complex microcontroller based circuits, the kit includes also several instrumental MMI models such as memories, interrupt generators, serial/parallel pattern generators, 7-segment displays etc. The Multifunction Model Interface (MMI) dialog for 8051 model supports following features:

- C Editor
- Assembly Editor
- Listing View
- Hex Editor
- Disassembler
- Output File
- Errors and Warnings

9. PIC Microcontroller Kit

The PIC kit includes main projects with assembler source code, which illustrates the functionality of PIC microcontrollers, with associated help files

The latest software version includes the PIC model and it's function libraries. The new MMI model for PIC allows coding in Assembler Editor and debugging them in real time while simulating with the rest of circuitry.

To facilitate analysis of more complex microcontroller based circuits, the kit also includes, several instrumental MMI models such as serial/parallel pattern generators, interrupt generators, 7-segment displays etc.

The PIC16C5x is the current version included in EDWinXP.

The Multifunction Model Interface (MMI) dialog for PIC model supports following features:

- Assembly Editor
- Listing View
- Hex Editor
- Disassembler
- Output File
- Errors and Warnings

10. AVR Microcontroller Kit

This kit includes example project databases designed to illustrate functionality of the simulation model for AVR AT90S2313 Microcontroller. Each project comes with associated help file that explains the example in details.

The new MMI model for AVR AT90S2313 allows coding programs in C or Assembler and debugging them in real time while functioning of the rest of circuitry is simulated.

Users can design complex microcontroller based circuits with the use of instrumental MMI models such as memories, interrupt generators, serial/parallel pattern generators, 7-segment displays etc.

The Multifunction Model Interface (MMI) dialog for AVR AT90S2313 Model includes the following modules:

- C Editor
- Assembly Editor
- Listing View
- Hex Editor (ROM)
- Hex Editor (EEPROM)
- Disassembler
- Output File
- Errors and Warnings

MM Simulation Model Generator

1. Analog Model Type

MM Simulation Model Generator enables to generate models of analog circuit elements. The logic function of analog elements may be very precisely described in so-called SPICE netlist format. Therefore the source for analog model generation is ASCII file containing SPICE sub-circuit.

PCB Layout Editor

1. New Autoplacer tools:

In Tools | Autoplace

Ø Relocate Component: Tool to relocate a component/ component text/ testpoints. There are options to rotate through 90 °, any angle, change the placement side, relocate component with name specified, swap components placement, toggle display of ratsnest/ trace/ outline etc. This

tool is defined in Tools | Components but has been included with the Autoplace tools for convenience.

∅ Relocate Block: Tool to relocate items selected in a block. There are options to rotate the block through 90°, through any angle, and to relocate items in the block including the board outline. This tool is defined in Tools | Block Edit but has been included with the Autoplace tools for convenience.

∅ Component and Net Property: Tool to view/change properties of selected component/component name, selected net, view a selected net on the Layout with its properties and to view the Schematic info of a selected net.

2. Component Browser

Customizable component browser has been introduced in Layout Editor. The browser embedded in Layout Editor provides the facility to browse and search for components.

3. Meshed Copper Pour Areas Display

This tool enables to view the meshed copper pour areas on a particular layer in the layout.

4. Multilayer copper pour connectivity check with 3D presentation included

Copper pour connectivity check, working in similar way as in Fabrication Manager, has been added to PCB Layout Editor. 3D presentation may be used to visualize detected errors on all layers where tested net connections are located.

5. Improved presentation of copper pours

On request, copper pour areas may be presented filled by meshed pattern for better visualization of boundaries on densely packed PCB layouts.

6. Auto Connect Functions

Auto-connect tools in Layout Editor are complement to manual trace routing tools. These auto-connect functions work directly on items in the project database. Execution time depends very much on the complexity of the board. Whether routing task is completed successfully depends on topology of currently existing connections.

The new Auto connect tools come under Tools | Connections | Auto Connect Traces are:

∅ Auto Connect Node Pair : Routing connection from node to node.

∅ Auto Connect Net: Routing connections for all nodes in selected net with the option to keep pre-routed traces unaltered.

Ø Auto Connect Net Element: Routing connection from selected net element (existing trace or node) to closest located element in the same net.

Ø Auto Lead-Out from Net Element: Routing lead-out traces from component nodes.

Ø Auto Clear Component Zone: Clearing a zone around a component(s) and re-routing all traces not connected to this component outside of the zone boundaries

Ø Auto Remove Vias: Removing redundant via holes on the whole board

Ø Auto Miter: Mitering all traces on the board in 45 degrees

Fabrication Manager

1. Improved multilayer copper pour connectivity check with 3D presentation

Previously implemented copper pour connectivity check has been enhanced for simultaneous testing of all artwork layers where connections for selected net are present. User may examine location of detected unconnected or isolated pads and isolated via holes with help of two or three dimensional presentation.

2. Polygonal copper relieve

Definition of areas on the artwork where copper should be removed from copper poured Gnd/Power planes was previously done through placing items like rectangles and circles. In present version relieve areas may be defined by polygons. A feature useful for removing of isolated islands of copper that usually have irregular shapes.

3. 3D export in IDF format

Feature allowing for exporting 3D view of the PCB in IDF Ver. 3 format

4. 3D IDF file viewer

Three-dimensional presentations of IDF Ver 3 format files.

Copper Removal Tools

5. Automatic Copper Cleanup

Enables removal of all "black" copper areas (isolated areas) from the artwork. The program analyses display of the artwork after test and generates copper relieve items in number and sizes necessary to cover all detected black spots.

6. Semi - automatic copper trimming

Enables to trim isolated "black" copper or connected "red" copper on the board. Trimming is necessary, especially when there are areas of connected (red) copper that are superfluous.

7. Polygonal Copper Relieve

Enables removal of isolated islands of copper that usually have irregular shapes (polygonal shape).

Library Editor

1. Triangular Package and Padstack

Allows to create triangular package and padstack.

3D Graphics

1. User definable true colors

Apart from 32 standard colors, the user may define custom palette of 224 colors and assign them to objects in three-dimensional visualization.

2. Improved scrolling and navigating

Current scroll position is retained when switching between 2D and 3D presentation. This is useful for examining results of connectivity check where alternating views without losing focus on the object is often required. Rotation of 3D view is executed around currently focused location rather than around coordinate system origin.

3. Semi-transparent view of copper pour areas and layout components

An extremely useful feature for 3D visualization of multi layered PCB designs.

General

1. Text Formatting:

Additional text formatting feature has been included in the Edit & Add Text Block dialog of Schematic Editor and Library Editor. This feature allows to add text of type Vector Font with an overline. e.g .

2. Import / Export Utilities:

This version of EDWinXP's Netlist/Wirelist Import and Export utility allows to import / export ALTERA EDF files to / from EDWin. It is also possible to convert EDWin Schematic Netlist to ALTERA EDF format and vice-versa.

What's new in EDWinXP 1.50

Following release of previous version, several new features and improvement to existing features have been implemented in EDWinXP 1.50

PCB Layout Design and Fabrication

1. Cooper pour connectivity test have been added PCB Layout Editor. Similar test was already included in Fabrication Manager. The advantage of this test in Layout Editor is that the connectivity may be checked while the board layout is designed. In both modules, the test may be now performed in selectable accuracy of 0.100, 0.050 and 0.025 mm. The time needed to execute the connectivity test has very significantly reduced.
2. Polygon shapes for copper removal introduced in 1.40, allowed to add feature that automatically removes unnecessary copper in isolated places within copper pour areas. This function was available for 1.40 users through live update. In 1.50, it has been improved in both speed (about 50% reduction of execution time) and accuracy.
3. Gerber View feature has been improved in order to reduce number of selections necessary to pre-process and display artworks in Gerber formats.
4. The option to plot inverted polarity circles and squares in size of pinholes for PMD component and vias has been added for Gerber format output. This option is available for in RS-274-X format only.
5. Settings for all fabrication exports (GenCAM, IDF and newly added Valor's ODB++ format) have been grouped in common dialog within Fabrication Manager.
6. It is now possible to import projects from other EDA packages in ODB++ format
7. Reconstruction of projects from Gerber format artworks been have significantly improved by adding feature for rebuilding component parts and packages from imported graphics. Projects can be now completely reconstructed even if necessary library elements are not available.
8. Number of tools for automatic routing of connection in PCB Layout Editor has been increased. It is now possible to automatically connect two separate trace branches of a net, re-route connections for a group of relocated components, route lead-out traces from pins of component with complicated pad patterns, automatically miter traces and remove redundant via holes.
9. Online clearance check has been introduced with improved visibility for detected clearance violations.

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10. It is now possible to display ratsnest in two modes: will all nodes or with unconnected nodes only.
 11. Important function "re-route" trace may be now performed in two modes: "re-route trace segment" and "re-route pin to pin connection. This latter is particularly useful when cleaning up design after auto-routing.
 12. Node marker size (squares) and pin entry marker size (crosses) are automatically adjusted to the pitch of component pads in order to ensure best visibility. Similarly, via hole marker size is automatically adjusted to smallest hole diameter in via pad stacks

Schematic Capture and Simulation

1. New feature called Filter Designer has been added. The system library includes prototype circuits for active low-pass, high-pass, band-pass and band-stop filters. Filter Designer allows to select one of the variants of those filters (Chebyshev, Butterworth, Bessel, Elliptic (Cauer) or Universal) and specify required filter output parameters – frequency and quality range. The parameters (capacitance and resistance) for filter circuit components are calculated and updated in the circuit, which subsequently may be appended to the project.
2. It is now possible to convert functional descriptions of discrete parts, expressed in form of SPICE format sub-circuit into analogue model for Mixed Mode Simulator.
3. Following code models have been added to MM Simulator and EDSPice model libraries:
4. New feature called Filter Designer has been added. The system library includes prototype circuits for active low-pass, high-pass, band-pass and band-stop filters. Filter Designer allows to select one of the variants of those filters (Chebyshev, Butterworth, Bessel, Elliptic (Cauer) or Universal) and specify required filter output parameters – frequency and quality range. The parameters (capacitance and resistance) for filter circuit components are calculated and updated in the circuit, which subsequently may be appended to the project.
5. It is now possible to convert functional descriptions of discrete parts, expressed in form of SPICE format sub-circuit into analogue model for Mixed Mode Simulator.
6. Following code models have been added to MM Simulator and EDSPice model libraries:

EDSPICE code models	MM Simulator models
M7218CD	DAC0800
MAX456	ADC0800
MAX4587	MAX232
MAX522	DAC AD 569

MAX5341	HPDL1414
MAX5352	ULN2003A
MAX625	STEPPER MOTOR
MAX690	POTENTIOMETER
MAX691	LCD DISPLAY
MAX696	LCD DISPLAY DRIVER-HD44780U
MAX697	.SWEEPGENERATOR.DLL
MAX701	
MAX702	
MAX708	
MAX7225	
MAX7240	

7. EDSPICE updates for EDWinXP 1.50

Sub-circuit files

- ? Diac
- ? CCCS
- ? CCVS

Circuit files (SPICE netlist format)

- ? BUCK CONVERTER AC MODEL.CIR
- ? DC_MOTOR_MODEL.CIR
- ? TREBLE AND BASS TONE CONTROLS.CIR
- ? I-TO-V CONVERTER (TRANSIMPEDANCE AMP).CIR
- ? CCCS.CIR

Sample projects with new EDSPICE sub-circuits

- ? 7805 Regulator - voltage regulator 7805
- ? CENTRE TAPPED TRANSFORMER - transformer
- ? Controlled Full Wave Rectifier - SCR
- ? OPTOCOUPLER- OPTOCOUPLER

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- ? IGBT - IGBT
 - ? Sidac characteristics - sidac
 - ? UJT Relaxation Oscillator – UJT
 - ? Current Controlled Current Source - CCCS
 - ? Current Controlled Voltage Source – CCVS

Updates in Part Libraries

PART	MANUFACTURER	SYMBOL	PACKAGE
0805AS-2N7M-01	Fastron	INDUCTOR	L/L70/SM
59S101-400E3	Rosenberger	CONN	CON/F5/A
74HC4052D	Philips	MUX4052	SOIC16/150
8516-4500	3M Interconnect Solutions	CONN	CON/HEADER16/A
8520-4500	3M Interconnect Solutions Division	CONN	CONN
CON/HEADER16/A			
8526-4500	3M Interconnect Solutions Division	CONN	CONN
CON/HEADER16/A			
8540-4500	3M Interconnect Solutions Division	CONN	CONN
CON/HEADER16/A			
8560-4500	3M Interconnect Solutions Division	CONN	CONN
CON/HEADER16/A			
A3953SB	Allegro	DRV3953	DIP16/300
ACSL-6400-T	Agilent Technologies	OPTO6400	
SOIC16/150			
ADF7020BCPZ1	Analog Devices	TxRx7020	LCC48/A
AT91SAM7S64	Atmel	MICR91SAM7S	
QFP64/D			
ATmega128L-8MC	Atmel	MICR128	LCC64
bq24022DRC	Texas Instruments	ADPTR24022	LCC10
BSP742T	Infineon technologies	SWT742	SOP8/150
C-551SR	Para Light	DISP5503	DIP10/600
CY8C27443-24PXI	Cypress	MCNTRLR8C27443	DIP28/300
DB15SRT/3R	Amphenol	CONN	
CON/DB15/D			
DCP010515DBP-U	Burr-Brown	DCP0105D	DIP14/300/P7

DS1822	Dallas Semiconductor	THERMO1822	TO92/3
dsPIC30F5011	Microchip	CNTRLR30F5011	
QFP64/C			
dsPIC30F6011	Microchip	CNTRLR30F6011	
QFP64/C			
dsPIC30F6014	Microchip	CNTRLR30F6014	
QFP80/B			
EP2C8F256	Altera	FPGA8C256F	
BGA256/e40			
F3345	FOX Electronics	XTALOSC1	
DIP4/SM/3			
FDC6301N	Fairchild	PFET_DG	SOT23/6
FDV303N	Fairchild	NFET_DG	SOT23/3
FSA4157P6	Fairchild	SPDT4157	SC88
G5V-2	OMRON	RLY1FORMC,RLY1FORM	
DIP16R/8			
GM5WA06260A	SHARP	LED	
DIP6/SM			
L5973D	ST Micro Electronics	VREG5973	
SOP8/150			
L6203	ST Micro Electronics	DRV6203	
TO220/11			
LAN91C111	SMSC	LAN91C111	
QFP128/C			
LATBT66C	OSRAM	3DIODE	DIP4/SM/B
LPC2106FBD48	Philips	MCNTRLR2106	QFP48
LZ-12VM	FUJITSU	RLY1FORMC	DIP5
M54562FP	Mitsubishi	DARARRAY54562	SOP20/200/A
MAX5400EKA-T	Maxim	DPOT5400	SOT23/8
MAX952ESA	Maxim	AMPR952	
SOIC8/150			
MC6802P	Motorola	MICR6802	DIP40/600
MC6821P	Motorola	ADAPTR6821	DIP40/600
MCF5235CVM100	Freescale	MICR5235	BGA256/e40
MIC2941ABU	Micrel	VREG2941	
TO263/5			
MM5450BN	Micrel	DRV5450	DIP40/600

MMA7260Q	Freescall	ACCLR7260	QFN16
MSC1202Y2RHHR	Texas Instruments	ADC1202	LCC36/A
nRF905-EVKIT 868/915	NORDIC	TxRx905	
LCC32/A			
PIC16F688I/SN	Microchip	MCNTRLR16F688	
SOIC14/150			
PIC16F876/SO	Microchip	MICR16F873	
SOIC28/300			
PIC18F4220-I/P	Microchip	MCNTRLR18F4220	
DIP40/600			
PIC18F452-I/P	Microchip	MCNTRLR18F442	
DIP40/600			
PIC18F452-I/PT	Microchip	MCNTRLR18F442	
QFP44/C			
PIC18F4550	Microchip	MCNTRLR18F4550	
DIP40/600			
PIC18F458-E/L	Microchip	MCNTRLR18F458	LCC44
QMB-111PC	Star	BUZZER	
PMD2/e12			
QT1080-ISG	Quantum	SENSOR1080	
LCC32/A			
RY-12	FUJITSU	RLY1FORMC,	RLY1FORM
DIP16R/8			
TA7252AP	Toshiba	AMP7252	SIP7/A
TDA7294V	ST Micro Electronics	AMP7295	TO220/15
TEL3-2422	Traco	CONV2422	DIP14/400/8
TLE5205-2GP	Infineon technologies	BRIDGE5205	
SOP20/425			
TLE6228GP	Infineon technologies	SWT6228	
SOP20/425			
TLE6232GP	Infineon technologies	SWT6232	
SOP36/400			
TLMK330	Vishay	LED	LCC2
TMP36FS	Analog Devices	SESON36	SOIC8/150
UC3906DW	Texas Instruments	ADPTR3906	SOIC16/300
ULN2004D	ST Micro Electronics	DARARRAY2003	SOIC16/150
XC9572	Xilinx	PLD9572	LCC44

TJA1040	PHILIPS	CANCNTR1040	SOIC8/150
LM317AMDT	NATIONAL	ADVOLTREG	
TO252/C			
FT232RL	FTDI Chip	UART232A	SOP28/200
2SA933AS	Rohm	PNP	TO202/3/B
2SC174S	Rohm	NPN	TO202/3/B
HD44780UA00TF	HITACHI	DISPCNTRLR44780	TQFP80
HD44780UA02TF	HITACHI	DISPCNTRLR44780	TQFP80

Symbol only parts

ANTENNA
 BUZZER
 CAVITYRESONATOR
 CIRCUITBREAKER
 COAXIALJACK
 CRO
 EARPHONE
 GALVANOMETER
 GUNNDIODE
 LAMP
 LASERDIODE
 LDR
 MICROPHONE
 MOTOR
 OHMMETER
 PHONEJACK
 PHOTODIODE
 PHOTOFET
 PHOTOVOLTAICCELL
 SCHOKELYDIODE
 STEPPERMOTOR
 THERMOCOUPLE
 TRIMMERCAPACITOR
 TUNNELDIODE
 VARACTORDIODE
 VARIABLECOIL
 WATTMETER